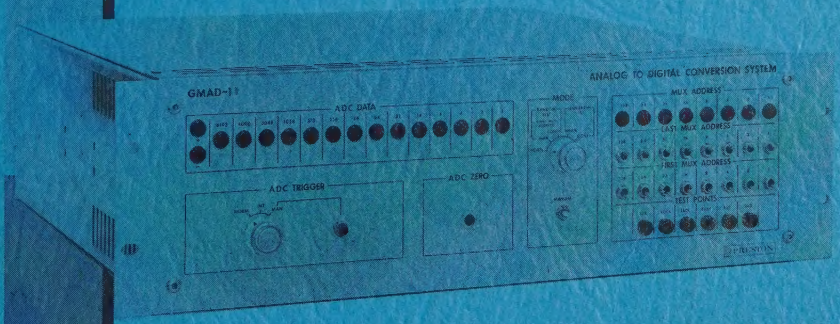
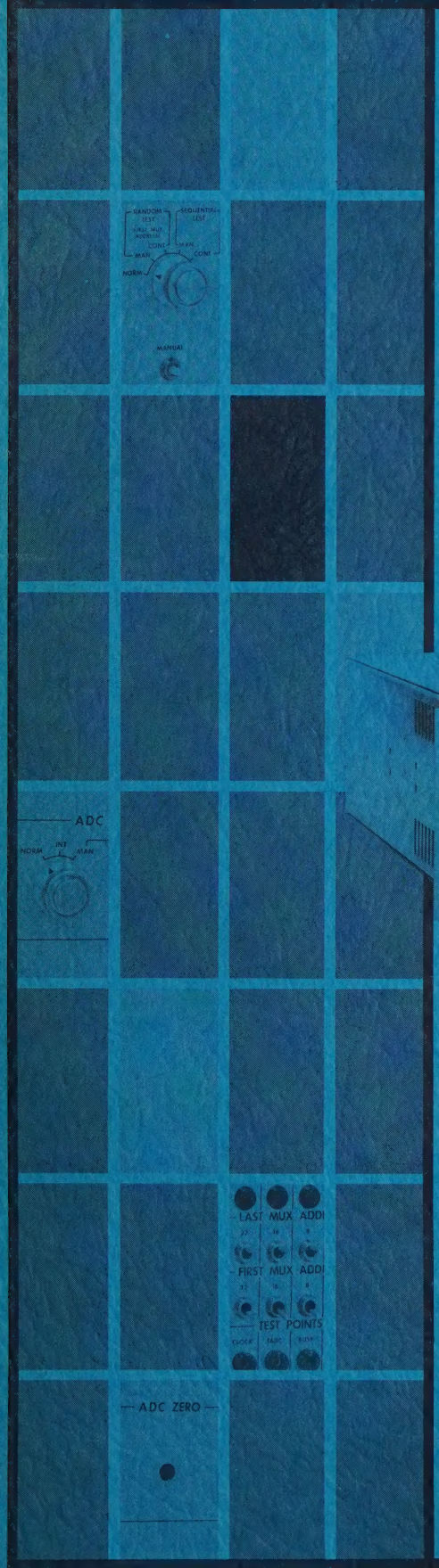
GM SERIES

ANALOG-TO-DIGITAL CONVERSION SYSTEMS

58855-01





PRESTON

GM SERIES

ANALOG-TO-DIGITAL

CONVERSION SYSTEM

SYSTEM PART NUMBER 58855-01

System Part Number 58855-01 Consists of.....

PART NUMBER 58700-03 A/D CONVERSION SYSTEM

and

PART NUMBER 58845-01 MULTIPLEXER EXPANDER

System of Record.....

PART NUMBER 58700-03 SERIAL NUMBER RAA-990

PART NUMBER 58845-01 SERIAL NUMBER RAB-004

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7133	CHANGED MANUAL TITLE PAGE TO REFLECT
	THE TOTAL SYSTEM DESCRIPTION
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	ADDED D#210V
7340	ADDED CLAMP PROCEDURE
	ADDED FIGURES 90114, 90119, 90120
8017	ADDED AMPLOGIC "ZCA" 54275
	ADDED ZERO CROSSING CONTROL 54280
	DELETED SIGN STORAGE 58710
8110	MODIFIED SYSTEM TO 58855-01
	NOW CONSISTS OF 58700-03 & 58845-01

INTRODUCTION

This document contains instructions for the operation and maintenance of the Preston GM Series Product noted on the title page.

The part number which describes this unit is located on the rear panel of the instrument. In addition, each unit is assigned a serial number unique to the particular piece of hardware to which it is attached. These numbers describe this instrument completely and should be referred to in all correspondence.

A complete replacement parts list is included in this manual, along with all drawings and schematics pertaining to the unit. The minimum spare parts order is $25.00. Prices quoted in the parts list are subject to change without notice.

Should the system need to be returned to Preston for repair or rework, the item should be sent to the Anaheim plant-- Attention: Customer Service-- and the shipping prepaid. Also, include reasonably complete information concerning the nature of the failure or your reason for the return of the equipment.

Our Address Is: PRESTON SCIENTIFIC INC.
805 East Cerritos Avenue
Anaheim California 92805

Our Telephone No. Is: (714) 776-6400

Our Telex No. Is: 65-5321

INTRODUCTION

SECTION 1

SYSTEM INTERFACE AND CONTROL

BASIC OPERATION INSTRUCTIONS

The Preston Analog-to-Digital Conversion System has a power requirement of 110-220 volts AC 50-60 Hz. The prime power requirement is customer specified and is noted both in the drawing section and the test report.

The GM System card modules are designed to be mounted into a standard 19-inch RETMA relay rack. To prevent damage to the front panel, nylon filler washers should be placed under the rack mounting screws. For correct weight distribution, drawer slides must be used for support. The unit has an integral fan. The ambient air should be maintained at less than 50 degrees centigrade.

Unless otherwise specifies the prime power is controlled by a rear panel ON-OFF switch and fuse. The value of the fuse is noted on the rear panel and also in the parts list.

ANALOG INPUT TERMINATIONS

Two types of multiplexers are employed by the GM Series System. The Model GMM is normally used for single-ended multiplexing applications. Some systems are configured using two GMM switches on each channel to provide a differential multiplexing capability.

The Model GMD series Amplifier-Multiplexer provides a differential amplifier per channel multiplexer capability for applications which demand intra-channel isolation. The Model GMD may be operated single-ended or differential depending upon the requirements of the customer.

SINGLE-ENDED INPUT MODEL GMM

When the Model GMM Multiplexer is used for single-ended applications, the input signal is connected between the channel input and analog ground (shield). The rear connector provides terminations for both of these connections for each channel. Please refer to the customer connection drawing in Section 11 and to the source and/or input impedance specifications for the multiplexer.

DIFFERENTIAL INPUT MODEL GMM

Differential input using the GMM Multiplexer is accomplished by using a pair of single-ended input multiplexer switches on each channel (please refer to the customer connection drawing for input termination pin

locations). You will note upon referring to the customer connection drawing, that the differential input is carried on three wires HI, LO, and SHIELD. The shield is not electrically terminated at the multiplexer switch, but does physically surround the input circuitry. The SHIELD must be referenced to the common mode source. The impedance between the HI or LO wires and multiplexer ground must not exceed the allowable specified source impedance of the multiplexer.

DIFFERENTIAL INPUT MODEL GMD

The input to the Model GMD Multiplexer is designed to be either differential or single-ended. The differential input uses a three terminal input, i.e. HI, LO and SHIELD, and all terminations are available at the rear connector. The SHIELD is not connected internally but does physically surround the input section of the multiplexer channel. The SHIELD must, however, be referenced to the Common Mode Source. The impedance between the HI or LO wires and GMD ground must not exceed 10 megohms.

COMMON MODE AND DIFFERENTIAL DRIVERS AND RECEIVERS

Leakage currents which are generated in the differential line receiver as noted in Figure 90004 must be returned to the power supply ground of the receiver. In Figure 90004, it will be noted that if point "X" at the receiver is not tied to its power ground, the leakage current has no path for return at the receiver end. This will cause some voltage to appear across resistance "R". If this voltage exceeds the common mode voltage limitations of the device, it will fail to operate properly. To prevent this common mode voltage from exceeding this limit, the resistance "R" is recommended to be less than 1K ohm.

In most systems there are line drivers and receivers communicating in both directions (between system and A to D). The ground return technique mentioned in the above paragraph is accomplished in the customers equipment. As indicated in Figure 90005, the power ground of the Driver "A" is connected to the power ground at Receiver "B" (point X1 to ground) at the customer side of the system. This connection is made via the resistance "R" (less than 1K ohm) and provides return for both Preston and customer receiver.

SYSTEM CONTROL

Control of the MUX/ADC System may be accomplished by any one of the following methods.

ALL EXTERNAL CONTROL (without optional GMC Logic Control Package)

Control signal input connections are provided for (1) binary channel address, no storage, (2) Sample-and-Hold commands (when applicable) and (3) Direct Trigger ADC (DTADC). When this method of control is used, all operations of the MUX/ADC combination are controlled by external means, all necessary settling times must be observed, and the channel addressing must not change during the conversion process

A timing diagram is supplied in Section 12 and contains the necessary information for the specific control signals and their proper timing sequence.

CONTROL USING AN EXTERNAL CLOCK (with optional GMC Logic Control)

For a complete description of the optional GMC Logic Control, refer to Section 3 of this Manual.

The optional GMC Logic Control Package permits the system to be operated in the external mode by either of the following two methods. In the external (NORMAL) Mode, a channel may be randomly addressed. When the ADD-X signal is HI, initiation of a CLOCK pulse will selec

the desired channel, and after the proper delays, will command the ADC to start the conversion process. No external Direct TADC is required. Also in the external mode (NORMAL), the front panel select switches of the GMC Control Logic are used to establish the first and last channels of a sequence of channels. When the ADD-X signal is LO and each clock pulse is received (externally provided), the next channel in sequence will be selected, followed by an automatic initiation of the conversion process. No external Direct TADC is needed in this mode.

SYSTEM CONTROL (with GMC Logic Control Package)

The following are some of the methods for system control via the Front Panel.

(a) Repetitious selection and conversion of the same channel by:

>>> placing the First MUX Address Switches on the desired channel

>>> placing the Mode Switch in RANDOM/MAN

>>> pressing the Manual Pushbutton (Multiplexer Control)

>>> placing the ADC/TRIGGER in INT (Internal).

As a result of the aforegoing 'set-up' the ADC will repetitively digitize the selected channel at a rate governed by the ADC Internal Clock (usually to 10 Hz).

(b) Repetitious conversion of the same channel may also be accomplished by:

>>> placing the Mode Switch in RANDOM/CONT (continous)

>>> placing the First MUX Address switches in the desired channel

>>> placing the ADC/trigger in the NORMAL position

As a result of this 'set-up', the ADC will repetitively digitize the selected channel at a rate governed by the Multiplexer Clock (usually at the maximum repetition rate of the converter/multiplexer combination).

(c) Repetitious conversion of the same channel 'manually' is accomplished by:

>>> placing the First MUX Address switches on the desired channel

>>> placing the Mode Switch in the RANDOM/MAN position

>>> pressing the Manual Pushbutton (Multiplexer Control)

>>> placing the ADC/Trigger in MAN

In the preceding configuration, the ADC will digitize the selected channel each time the Manual pushbutton (ADC Control) is depressed.

(d) Sequential selection and conversion of a series of channels manually by:

>>> placing the mode Front Panel Switch in SEQUENTIAL/MAN position

>>> placing the First MUX Address switches to the first channel desired

>>> placing the Last MUX Address switches to the last channel desired

>>> placing the ADC/trigger in the NORMAL position

In this 'set-up' pressing the Manual button (Multiplexer Control) will select each channel one at a time and convert that channel.

(e) Sequential selection and conversion of a series of channels

automatically by:

>>> placing the Mode Switch in the SEQUENTIAL/CONTINUOUS position

>>> placing the First MUX Address switches to the first channel desired

>>> placing the Last MUX Address switches to the last channel desired

>>> placing the ADC/Trigger in the NORMAL position

The preceding allows the control system to advance through and convert each channel in sequence at a rate governed by the multiplexer control clock (usually at the maximum repetition rate of the Multiplexer/ADC combination).

SAMPLE-AND-HOLD CONTROL LOGIC

Each one of the sample-and-hold boards has its own control logic. The logic diagram is pictured in Figure 90006. Refer to the chart in Figure 90007 for the different ways to control the sample-and-hold modes and their subsequent logic connections.

Common types of control are:

(a) A pulse on the sample line to obtain the sample mode, and a pulse on the hold line to obtain the hold mode

(b) Single line drive sample logic line

(c) Single line drive, hold logic line, true for hold, false for

sample.

SECTION 2

MULTIPLEXER

MODEL GMM

FUNCTIONAL DESCRIPTION (Figure 90008)

The GMM Multiplexer is a single-ended input/single-ended output semiconductor device. Some systems use this device as a differential multiplexer by using a pair of GMM Multiplexer switches for each differential channel involved, followed by either a differential buffer or Sample-and-Hold Amplifier.

Figure 90008 is an over-all block diagram of the GMM Multiplexer in a system application. Analog input signals are connected to the multiplexer channels from the rear connectors by shielded cabling. Each multiplexer circuit board contains four multiplexer switches, associated switch drive control logic, and analog overload clamps. Control of the multiplexer may be directed from the front panel optional GMC Logic Control Package (see Section 3 and Figure 90008) or by the customer interface at the rear panel connectors (refer Section 1).

SPECIFICATIONS

TYPE: Single-ended SPST

CHANNEL SELECTION: Selection by random address, sequential or any combination of both, when the GMC Logic Control Package is employed.

SWITCHING TIME: Less than 1 microsecond.

ACCURACY: 0.01%

INPUT IMPEDANCE: Greater than 50 megohms.

CROSSTALK: Between channel crosstalk is less than 0.01% of full scale

LINEARITY: 0.01% of full scale.

ZERO DRIFT: Less than +/-1.0 millivolt.

LOGIC LEVELS: Either positive or negative true.

OPERATING INSTRUCTIONS

The System Multiplexer may be totally external controlled by the customer or may be controlled by the optional GMC Logic Control Package. A description of these control methods appears in Section 1 and 3 of this manual.

THEORY (Figure 90009)

The multiplexer switch is a Field Effect Transistor (FET). Figure 90009 shows channel address circuit and a FET switch circuit. Each of the GMM Multiplexer boards contain four identical FET switch circuits, one for each of the four channels. Because the FET has no inherent offset voltage, whatever signal is on the input will also appear on the output (when the switch is turned ON). One characteristic of the FET used in the GMM Multiplexer is that it is normally ON with zero gate voltage and is turned OFF by the application of a voltage having negative polarity. Also shown in Figure 90009, the analog channel input is connected to the Drain (D) and the multiplexer output is connected to the Source (S) of the FET. When the voltage between the Drain and the GATE (G) is Zero, the FET will conduct and the Source will be brought to the potential of the Drain.

To turn off the FET, the Gate must be clamped to a negative voltage. To insure that the Gate will obtain the same potential as the Drain and the FET will turn on in the shortest amount of time when the Gate is released, the input of a unity gain amplifier (see Figure 90010) is

tied to the Drain of the FET and the output of the unity gain amplifier is tied to the Gate of the FET. This added circuit increases the slewing rate of the FET Gate.

The multiplexer switch and its unity gain amplifier appear in block diagram form in Figure 90011.

AMPLIFIER MULTIPLEXER

MODEL GMD-1

LOW GAIN

FUNCTIONAL DESCRIPTION MODEL GMD

The Model GMD Amplifier Multiplexer is a Differential Input Amplifier followed by a single-ended input/single-ended output semiconductor switch.

Figure 90080 is an over-all Block Diagram of the Model GMD Multiplexer in a system application. Analog signals are connected to the multiplexer channels by shielded cabling. Each multiplexer board may contain one or two multiplexer channels, associated drive control logic and analog overload clamps. The number of channels per circuit board is determined by the particular system application.

Control of the multiplexer channels may be directed from the front panel (Optional GMC Logic Control Package, see Section 3 and Figure 90080) or by the customer interface at the rear panel connectors (refer to Section 11).

SPECIFICATIONS MODEL GMD-1

AMPLIFIER TYPE : Direct coupled fixed gain

GAIN: The gain of the amplifier is fixed single gain between 1 and 5 for the Model GMD-1 and at one-tenth (0.1) for the Model GMD-01.

GAIN ACCURACY: +/-0.01% of full scale

GAIN STABILITY: +/-0.01% of full scale for six months at the same temperature

GAIN TEMPERATURE COEFFICIENT : Less than +/-0.002% per degree C

GAIN TRIM: Permits adjustment to within 0.01%, resolution is 0.005% or better.

DC LINEARITY: Maximum deviation +/-0.01% of full scale.

ZERO STABILITY: Short term +/-0 5 millivolts RTO (Relative to Output) for 48 hours at the same temperature.

ZERO TEMPERATURE COEFICIENT: +/0.05 millivolts RTO per degree C

ZERO TRIM: A zero offset adjustment is provided with resolution of 0.1 millivolts.

INPUT IMPEDANCE: 100 megohms for the Model GMD-1, 100 k ohm for the Model GMD-01.

SHUNTING CAPACITANCE: 100 picofarads.

COMMON MODE REJECTION: 80 dB from DC to 60 Hz.

COMMON MODE VOLTAGE:* 10 volts peak AC or DC for balanced inputs, 5 volts peak for signal-ended inputs.

PUMPOUT CURRENT: 10 picoamps nominal.

INPUT CONNECTION: Requires only three wires: Input High, Input Low and Guard.

INPUT OVERLOAD RECOVERY:* The amplifier will recover from an overload of two times full scale to within +/-0.05% of full scale in less than 200 microseconds. Recovery time of the amplifier increases proportionately as the bandwidth decreases (i.e., at 1 kHz, recovery time is 2 milliseconds).

OUTPUT MULTIPLEXED:** Commutated +/-10 volts full scale.

OUTPUT IMPEDANCE-ON: 500 ohms maximum.

OUTPUT LEAKAGE CURRENT-OFF: 15 nanoamps maximum.

CROSSTALK: 0.01% of full scale maximum for 100 channels

SWITCHING TIME: 1 microsecond to 0.01% of full scale into a load of 10 megohms shunted by 500 pf (analog bus should be guarded and driven externally if wiring capacity exceeds 500 pf or if insulation exhibits dielectric absorption).

FAULT CONDITION: The multiplexer switch is protected against fault condition of the amplifier.

BANDWIDTH: Less than 3 dB down at 1 MHz at 10 volts peak-to-peak.

OPTIONAL FILTER: Any fixed bandwidth from 10 Hz to 1 MHz.

SETTLING TIME: 2.0 microseconds maximum to within 0.01% of final value +/-10 microvolts RTI at 1 MHz. Settling time of the amplifier increases proportionately as the bandwidth decreases (i.e. at 1 kHz, settling time is 2 milliseconds).

NOISE CHARACTERISTICS: Output noise is less than 1.0 millivolts peak-to-peak, typically 0.5 millivolts peak-to-peak.

*The voltage levels referenced in these specifications should be multiplied by 10 when applied to the GMD-01 Amplifier-Multiplexer.

**A direct Output of the GMD Amplifier is available upon special request This output is electronically located before the MUX Switch

input.

OPERATING INSTRUCTIONS MODEL GMD-1

The System Multiplexer may be totally controlled by the customer or may be controlled by the Optical GMC Logic Control Package. A description of these control methods appear in Sections 1 and 3 of this manual.

THEORY (Figure 90081) MODEL GMD-1

The Multiplexer Switch is a Field Effect Transistor (FET). Figure 90081 shows the channel address circuit and the FET switch circuit. Because the FET has no inherent offset voltage, whatever signal is on the input will also appear on the output (when the switch is ON). One characteristic of the FET used in the Model GMD Amplifier Multiplexers is that it is normally ON with ZERO GATE voltage and is turned OFF by application of a voltage having negative polarity.

Also shown in Figure 90081, the output of the GMD Amplifier is connected to the DRAIN (D) and the multiplexer output is connected to the SOURCE(S) of the FET When the GATE is released from its negative potential and assumes the potential of the DRAIN, the FET will turn ON and the SOURCE will be brought to the potential of the DRAIN.

The Multiplexer Switch and its input amplifier appear in block diagram form in Figure 90082.

CALIBRATION MODEL GMD-1

COMMON MODE ADJUSTMENT

(a) Tie the input HI and input LO together.

(b) Apply a 20 volt, 60 Hz, AC signal between the tied-together inputs and ground.

(c) Observe the test point marked AMP OUT. Adjust the CM potentiometer for minimum output (20 millivolt scale).

ZERO

Short the input of the multiplexer and adjust the ZERO potentiometer for a zero reading on the ADC readout (within the accuracy of the system).

GAIN

Regardless of the Gain of the GMD Amplifier, the output is usually 10 volts in order to be compatible to the ADC full scale. Each individual system will have its own gain requirement per customer specification (see Section 5 for System Specifications).

(a) Determine the input required to obtain a Full Scale reading on the ADC readout.

(b) Introduce the input between the HI and LO input of the GMD Multiplexer.

(c) Adjust the gain potentiometer to obtain a full scale reading on the ADC output.

Check the ZERO and GAIN adjustments again and make the necessary adjustments.

AMPLIFIER MULTIPLEXER

MODEL GMD-10/1000

HIGH GAIN

FUNCTIONAL DESCRIPTION MODEL GMD-10/1000 (Figure 90080)

The Model GMD Amplifier Multiplexer is a Differential Input Amplifier followed by a single-ended input, single-ended output semiconductor switch.

Figure 90080 is an over-all Block Diagram of the Model GMD Multiplexer in a system application. Analog signals are connected to the multiplexer channels by shielded cabling from the rear connector. Each multiplexer board contains, one amplifier, one multiplexer switch, associated drive control logic and analog overload clamps.

Control of the multiplexer channels may be directed from the front panel (optional GMC Logic Control Package, see Section 3 and Figure 90080) or by the customer interface at the rear panel connector (refer to Section 11).

SPECIFICATIONS MODEL GMD-10/1000

The specifications set forth in the following sections should be combined with the A/D Converter specification (refer to Page 8 of the GM Series A/D Conversion System brochure) in arriving at a total system performance specification.

GAIN: One fixed gain within the range of 10 to 1000, customer specified.

GAIN ACCURACY: +/-0.01%.

GAIN STABILITY (at constant temperature): +/-0.01%.

GAIN TEMPERATURE COEFFICIENT: 20 ppm/C.

LINEARITY: +/-0.01%.

ZERO STABILITY: 10 microvolts RTI and 1 millivolt RTO for 48 hours

ZERO TEMPERATURE COEFFICIENT: 1 microvolt/C RTI and 0.05 millivolt/C RTO.

INPUT IMPEDANCE: 10 megohms.

SHUNTING CAPACITANCE: Selected for system requirements. *(Normally 1 nanofarad)

*Depends on source impedance and data bandwidth requirements.

COMMON MODE REJECTION: 60 dB + gain or 108 dB DC to 60 Hz (whichever is smaller).

COMMON MODE VOLTAGE: 10 volts peak AC or DC for balanced inputs, 5 volts peak for single-ended inputs.

PUMPOUT CURRENT : 10 nanoamperes.

INPUT CONNECTION: Three wires --- Input high, inpút low and input guard.

NOTE: The signal source must not be floating. It may have no more than 10 megohms impedance to ground.

NORMAL MODE VOLTAGE: 20 volts maximum.

INPUT OVERLOAD RECOVERY: From input transition of +/-5 volts to 0 volts in less than 1 millisecond to 0.01% FS +/-10 microvolts RTI at full bandwidth

CROSSTALK: Less than 0.01% +/-3 microvolts RTI for 100 channels.

BANDWIDTH: -3dB at 20 kHz

SETTLING TIME: From +/-FS to 0 volts in less than 250 microseconds to

OPERATING INSTRUCTIONS MODEL GMD-10/1000

The Multiplexer may be totally controlled by the customer or may be controlled by the optional GMC Logic Control Package described in Section 3. A description of these control methods appear in Sections 1 and 3 of this manual.

THEORY (Figure 90083) MODEL GMD-10/1000

The multiplexer switch is a FET (Field Effect Transistor). Figure 90083 shows a schematic of the GMD Amplifier Multiplexer displaying the channel address circuit, amplifier, and the FET switch circuit. Because the FET has no inherent offset voltage, whatever signal appears on the input will also appear on the output (when the switch is ON). One characteristic of the FET used in the Model GMD is that the switch is normallly ON with a ZERO gate voltage and is turned OFF by the application of a negative voltage of significant value applied to the gate.

Also shown in Figure 90083, the output of the GMD Amplifier output is connected to the DRAIN (D) and the multiplexer output is connected to the SOURCE (S) of the FET. When the gate is released from its negative potential and assumes the potential of the DRAIN, the FET will turn ON and the SOURCE will be brought to the potential of the DRAIN.

The multiplexer switch and its input amplifier appear in Block Diagram form in Figure 90082.

CALIBRATION MODEL GMD-10/1000

ZERO ADJUSTMENT

(a) Short the input HI and LO of the amplifier multiplexer to ground.

(b) Adjust the ZERO potentiometer for a zero reading at Pin 15.

(c) Measure the output of Pin 17. This value should be within a millivolt of the reading at Pin 15. If the difference exceeds 1 millivolt, perform the resistor selection as per Note 5 of the drawing.

PUMPOUT CURRENT ADJUST

(a) With the HI and LO input of the Amp/MUX shorted to ground insert a 10K ohm resistor in the LO input.

(b) Adjust the IBL potentiometer to return the post filter ouptut (pin 17) to zero.

(c) Move the 10K ohm resistor to the HI input and adjust the IBH potentiometer to return the post filter output to zero.

COMMON MODE ADJUST

(a) Tie the input HI and LO together.

(b) Apply a 20 volt, 60 Hz signal between the tied together inputs and ground.

(c) Observe the pre-filtered output at pin 15 and adjust the CMR potentiometer for a minimum output.

(d) Different gains have different criteria for the common mode final setting. Below is a list of the gain of the amplifier and the corresponding allowable reading.

GAIN	ALLOWABLE READING
1000	80 millivolts p-p
500	40 " "
200	20 " "
100	20 " "
50	20 " "
20	20 " "
10	20 " "

GAIN (Figure 90084)

(a) Connect the AMP/MUX channel as indicated in Figure 90084.

(b) Adjust the gain potentiometer to obtain a horizontal line on the oscilloscope. When the line on the scope has no slope the gain is adjusted properly.

(c) Check the common mode voltage, zero, and gain settings and make any necessary adjustments.

SECTION 3

GMC LOGIC CONTROL SYSTEM

INTRODUCTION

When the optional GMC Logic Control is included in the MUX/ADC combination, the system may be operated in many different modes. A basic introduction to the modes of operation appears in Section 1 of this manual. The following series of paragraphs gives a functional description for the switches and controls located on the front panel.

FIRST ADDRESS

Selection of single channel address when MODE Switch is in RANDOM TEST, MAN or CONT; Selection of the first channel in a series when the MODE Switch is in NORMAL, SEQUENTIAL TEST, MAN or CONT.

LAST ADDRESS

Selection of the last channel when the MODE Switch is in NORMAL, SEQUENTIAL TEST, MAN or CONT.

MODE SWITCH

(a) NORM (Normal) --- In this position, the primary control of the multiplexer is at the customer's command via the rear connectors.

(b) RANDOM TEST --- Relates to the FIRST MUX ADDRESS only. When the MODE Switch is on the RANDOM TEST-MAN position, depressing the MANUAL button will select the channel indicated by the FIRST MUX ADDRESS. When the MODE Switch is in the RANDOM TEST CONT position, the control will automatically and continuously select the channel indicated by the FIRST MUX ADDRESS.

(c) SEQUENTIAL TEST --- This position incorporates both FIRST MUX ADDRESS and LAST MUX ADDRESS switches. When the MODE Switch is in the SEQUENTIAL TEST-MAN position, depressing the manual button will select, in order, the channels between and including FIRST and LAST MUX ADDRESS. Turning the MODE Switch to the SEQUENTIAL TEST-CONT position will allow an internal clock to sequence through the channels between and including the channels indicated by the FIRST and LAST MUX ADDRESS switches.

TEST POINTS --- Monitoring points only for specified signals of interest. In the standard configuration, the following signals may be monitored from the front panel test points: EXAD, COIN, CLOCK, BUSY, GND, and TADC.

INPUT CONTROL LINES (REAR PANEL CONNECTOR)

The following is a list of input control lines associated with the GMC Control System.

ADDRESS ---- This is a multiplexer channel binary address externally furnished to randomly select a particular multiplexer channel. A TTL compatible binary word of four or more bits in length is required. This address is only effective when the front panel GMC Control Package MODE Switch is in the NORMAL position.

CLOCK (CLK) --- The CLOCK function is an externally furnished TTL pulse, 100 nanoseconds minimum width, which is used in conjunction with the (ADD-X, EXAD) function to (1) gate in the random binary address or (2) advance the multiplexer to the next channel. The CLOCK function also sets the proper delays to initiate the A/D Conversion process.

EXTERNAL ADDRESS (EXT ADD)---The EXT ADD function is a TTL level which establishes the mode of operation for the external CLOCK function. When the EXT ADD level is true the CLOCK function will be used to gate in the random channel address from an external i.e.,---and when the lever is false, the CLOCK function will be used to sequentially advance the multiplexer channels within the limits established by the front panel MUX address switches. The EXT ADD function is effective when the front panel CMC Logic Control System MODE switch is in the NORMAL position.

When sequentially advancing to the channel selected by the LAST MUX ADDRESS switches, the next CLOCK pulse will cause the channel indicated by the FIRST MUX ADDRESS switches to be selected.

RESET---The RESET function is an externally furnished TTL level, used to reset the internal register to the channel selected by the front panel FIRST MUX ADDRESS switches. Application of the RESET and CLOCK function will initiate a return to the channel selected by the FIRST MUX ADDRESS switches. Reset does initiate a conversion of the first channel. When the RESET function is not being used, it should be tied to the digital ground.

OUTPUT CONTROL LINES

NORMAL MODE---The NORMAL MODE function relates to the position of the front panel MODE switches for either or both the ADC and the multiplexer. When both of these front panel switches are placed in the NORM position, the signal on the designated pin of the rear connector (see customer connection drawing in Section 11) will appear as a TTL level HI with reference to ground. If either switch is changed to another position, the signal at the rear connector will appear as a TTL level LO.

END of SCAN (COIN)---The COIN function is a TTL level which becomes "true" upon selecting the "last channel" for digitizing as established by the front panel address.

BUSY---Indicates that the system is BUSY. Refer to the Test Report for the specific timing.

EOC---The A/D Converter will also provide a separate EOC function as indicated that the conversion is complete and the data lines have settled. This appears as a TTL pulse 100 nanoseconds minimum width The EOC function may be used as an output data strobe.

SECTION 4

ANALOG-TO-DIGITAL CONVERTER

MODEL GMAD

FUNCTION DESCRIPTION

The Model GM Series Analog-to-Digital Converter is a solid state device that will upon command produce a binary digital representation of an analog input signal.

The digital output of the ADC is presented in a parallel binary word. The output code is customer specified. For full scale, conversion speed, accuracy, and timing, refer to the Test Report in Section 10.

The speed of the conversion or throughput rate varies with the model and resolution of the converter. The inclusion of a Sample-and-Hold Amplifier and/or multiplexer channels also effects the total conversion time of the system. Specifications located in this section are for the ADC only and do not represent the system operation. Refer to Section 5 of this manual for unique specifications concerning the entire system.

SPECIFICATIONS GMAD 1

CONVERSION RATES :

14 binary bits and sign	750 kHz
13 binary bits and sign	760 kHz
12 binary bits and sign	800 kHz
11 binary bits and sign	1 MHz

CONVERSION TIMES :

14 binary bits and sign	1.5 microseconds
13 binary bits and sign	1.4 microseconds
12 binary bits and sign	1.2 microseconds
11 binary bits and sign	1 microseconds

INPUT IMPEDANCE : 100 megohms or greater

SOURCE IMPEDANCE : 100 ohms maximum

DATA OUTPUTS : TTL

OUTPUT CODE :

(a) BINARY

True bipolar

One's Complement

Two's Complement

(b) BCD

True bipolar

Nine's Complement

Ten's Complement

ACCURACY :

14 binary bits and sign	+/-0.01%	+/-1/2 LSB
13 binary bits and sign	+/-0.015%	+/-1/2 LSB
12 binary bits and sign	+/-0.025%	+/-1/2 LSB
11 binary bits and sign	+/-0.05%	+/-1/2 LSB
10 binary bits and sign	+/-0.1%	+/-1/2 LSB
9 binary bits and sign	+/-0.2%	+/-1/2 LSB
8 binary bits and sign	+/-0.4%	+/-1/2 LSB
7 binary bits and sign	+/-0.8%	+/-1/2 LSB

INPUT VOLTAGE RANGE : Standard ranges are from +/-10 volts. Other ranges are available upon special request.

DIGITIZE COMMAND : Positive or negative slope and pulse width greater than 10 nanoseconds.

END-OF-CONVERSION : Parallel data ready indication, nominal pulse duration is 100 nanoseconds.

POWER : The ADC systems are equipped with their own integral DC power supply and require only standard line voltage (115v AC +/-10% 60 Hz).

SAMPLE-AND-HOLD GMSH-10 AND GMSH-100

GAIN : 1.000 +/-0.01%

GAIN STABILITY and LINEARITY : +/-0.01% of full scale

INPUT IMPEDANCE : Greater than 100 megohms.

SOURCE IMPEDANCE : 0 to 1000 ohms.

OUTPUT IMPEDANCE : Less than 1 ohm.

OUTPUT LOAD : 200 ohms minimum, 500 pf maximum.

SETTLING TIME (acquisition time to 0.01%) SAMPLE MODES :

(a) GMSH-10 :

0.5 microseconds from one full scale polarity to the opposite polarity (10 volts full scale)

(b) GMSH-100 :

2 microseconds from one full scale polarity to the opposite polarity (10 volts full scale).

HOLD DELAY

(a) GMSH-10 : 0.25 microseconds after HOLD pulse leading edge.

(b) GMSH-100 : 1 microsecond after HOLD pulse leading edge.

HOLD APERTURE

(a) GMSH-10 : 10 nanoseconds

(b) GMSH-100 : 50 nanoseconds

NOISE : 0.5 millivolts peak

DROOP IN HOLD MODE : +1 millivolt after 1 millisecond.

OPERATING TEMPERATURE : The converter will perform to the specifications stated, within a temperature range of 0C to +50C.

COOLING : For proper operation, the air surrounding the converter should be maintained between 0C and +50C, with a relative humidity note to exceed 70%. The converter utilizes its own fan for internal cooling.

STORAGE CONDITIONS : The converter will show no deterioration when subjected to storage temperatures of -55C to +85C and to relative humidities of up to 100% without condensation.

SIZE : The dimensions of the converter are 20 or 26-1/2 inches in length (total), 19 inches in width and 5-1/4 inches in height.

WEIGHT : The converter weighs 45 - 55 pounds (shipping weight is 60-75 pounds).

MOUNTING : The converter will mount into a standard 19-inch RETMA Rack.

OPERATING INSTRUCTIONS

The system operation of the GM Series ADC is covered in Section 1 and Section 3. Special system sequencing or operations may be found in Section 5 System Description.

ADC Front Panel Controls

Three controls related to the ADC in the system are located on the front panel. These are ADC TRIGGER FUNCTION SWITCH, ADC TRIGGER PUSHBUTTON SWITCH, and ADC ZERO. The ADC TRIGGER FUNCTION SWITCH has three positions :

NORM (Normal) position : This position is used when the ADC is being triggered by the systems GMC Logic Control Package (See Sections 1 and 3).

INT (Internal) : This position provides constant asynchronous conversion of the analog input at a rate determined by an internal clock located on the ADC timing circuit board (Clock frequency is typically 10 Hz).

MAN (Manual) : Placing the function switch in this position will allow a new conversion to be initiated each time that the ADC PUSHBUTTON SWITCH is depressed.

The ADC ZERO is a recessed screwdriver adjustable potentiometer to

allow for the correction of zero offsets that may be caused by peripheral equipment.

THEORY

The GM Series Analog-to-Digital Converter consists of a series of similar bit boards. Each bit board consists of two basic elements. These elements are : (1) an analog circuit for each individual bit and (2) a logic storage and decoding section for each individual bit (refer to Figure 90012).

In the GM Analog-to-Digital Converter, several of the above described bit boards are connected in series as indicated in Figure 90012, and each circuit receives, as its input, the output of the preceding circuit.

Each individual analog circuit is identical in operation. Schematically, the bit board (printed circuit) part values will change from the MSB to the LSB due to the decreased resolution of each successive bit board.

Using the block diagram in Figure 90012, note that each bit board, including the sign, has its own analog circuit and logic storage. The buffer is used to provide a high impedance to the source.

Each converter has the same transfer function as indicated in Figure 90013. If the "X" axis is the input signal of each of the analog circuits, then the "Y" axis in the resultant analog output of the circuit, e.g., as the input varies from minus 10 volts to plus 10 volts, the resultant output of the analog circuit will vary from plus 10 volts to minus 10 volts and back to plus 10 volts.

The logic storage stage is designed to give a logic output as follows: For all positive inputs to the analog circuit, the logic output will be a "0" and for all negative inputs, the logic output will be "1".

Figure 90014 shows the operation of a minus 10 volt to plus 10 volt signal and the subsequent outputs of each amplifier, along with the logic ("1" or "0"). For positive inputs, a logic "0" is realized and for negative inputs, a logic "1" is realized. In this manner, a Gray code logic may be obtained as a representative digital value of the input to the ADC.

The ADC operates in the Gray code rather than normal binary because this allows the progression of the code to advance only one bit at a time. To convert the Gray code into normal binary, the storage and decoding sections (see Figure 90014) use the following process:

> Starting with the MSB, which is connected to give a binary output that is the complement of the Gray code, each time a bit board is preceded by data output that is a "1" logical, that bit is reversed ("0" to a "1" and vice-versa). See the binary and Gray

codes in Figure 90014 for an example.

The GM Analog-to-Digital Converter follows the input signal at all times. To receive a digital representation of the input at any time, all that is necessary is to gate the storage sections simultaneously The logic is then converted from a Gray code to binary and released to the output.

BIT BOARD DESCRIPTION

Figure 90015 is a block diagram of a bit board, the fundamental building block of the converter. The diagram includes the input amplifier (A1), the output amplifier (A2), the zero crossing detectors, the logic storage and decode logic.

Amplifier A1 output is connected to the zero crossing detectors and, depending upon whether the input to the amplifier is negative or positive, sets the logic of IC A3. The logic of IC A3 is stored at IC A3 when the GATE pulse is received. When the GATE pulse is received (the GATE pulses are also named UPDATE ADC and may be observed at the control board on test points marked DELAY 1 and DELAY 2), the logic is transferred to the IC's A1 and A2. Through interconnection with the subsequent and preceding bit boards, the Gray code is converted into the correct binary output. The output of Amplifier A2 is fed to the input of the next bit board and the above process is repeated. In operation, when all of the bit board's logic is settled the GATE pulse is applied and the binary digital representation of the analog input

appears at the output and is displayed on the front panel.

C Y C L I C C O N V E R S I O N T E C H N I Q U E

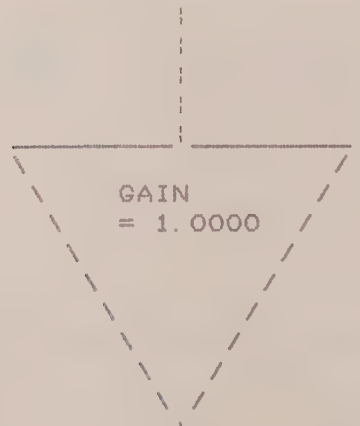
TYPICAL BLOCK DIAGRAM FOR GMAD-1,2,3 CYCLIC A/D CONVERTERS.
NOTE THAT ACTUAL ANALOG INPUT IS OFFSET BY 1/2 LSB
THIS OFFSET IS TAKEN OUT WITH THE BUFFER OR SAMPLE-AND-HOLD
IN FRONT OF THE ADC

NOTE: THE LAST 4 BITS ARE NOT ACTUALLY MECHANIZED IN THE
SHOWN AS ONE BIT PER BOARD BUT THE RESULTS ARE THE SAME
THE LAST 4 BITS ARE GENERATED ON THE 4 BIT AMP AND 4 BIT
LOGIC BOARDS NOT THE TYPICAL AMP-LOGIC BOARDS SHOWN.

IF THE FULL-SCALE INPUT TO THE BUFFER OR S & H
IS 10.0000 VOLTS ,

AND

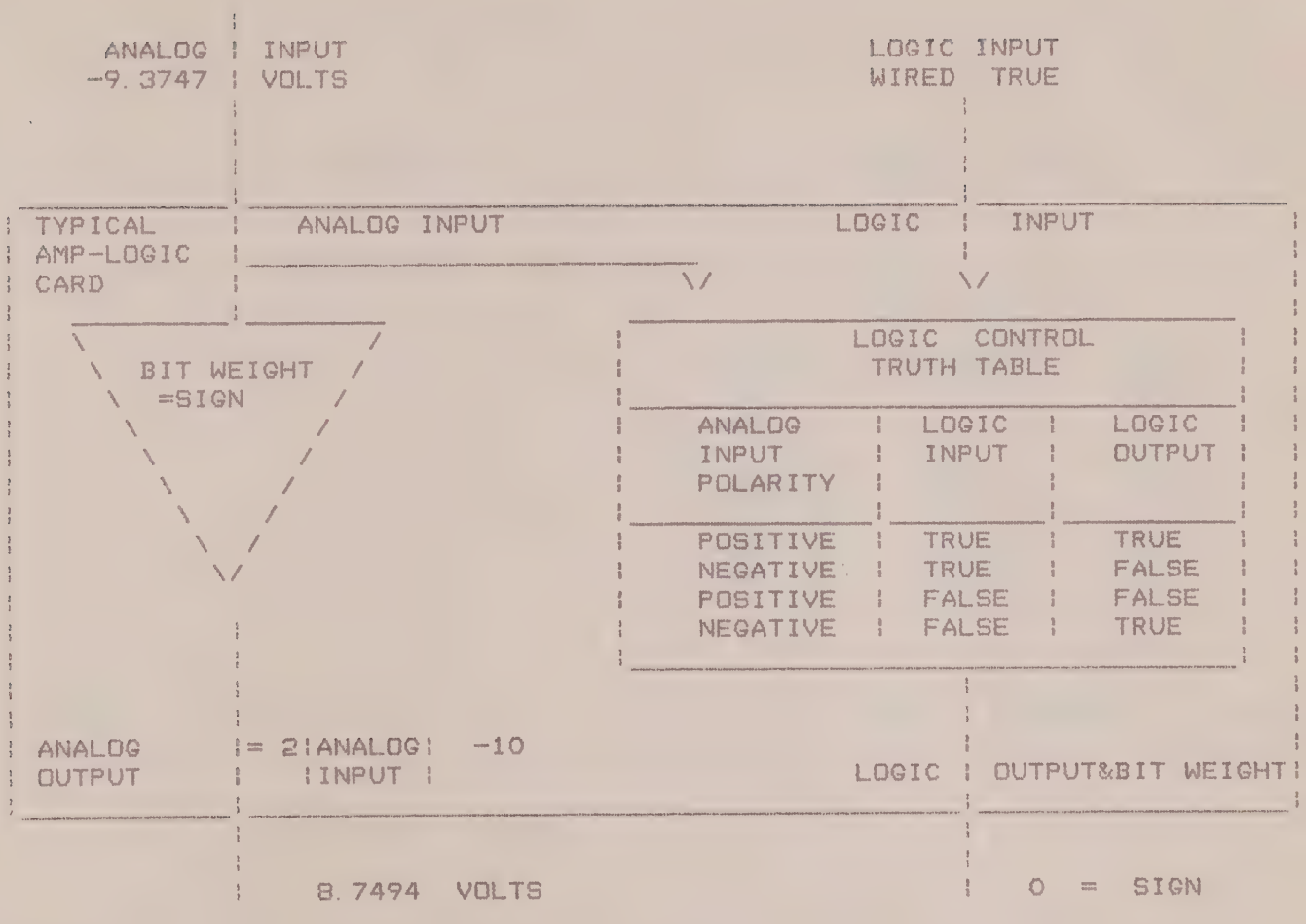
IF THE INPUT VOLTAGE INPUT IS -9.3750 VOLTS



BUFFER OR SAMPLE-AND-HOLD

OUTPUT = -9.3747 VOLTS;
THIS INCLUDES +0.00031 VOLTS OFFSET
WHICH IS EQUAL TO 1/2 LSB (REFERRED TO THE THE BUFFER OR
SAMPLE-AND-HOLD OUTPUT) WHICH IS SCALED
FOR 10.0 VOLTS WITH A FULL-SCALE INPUT.

THE BUFFER OR SAMPLE AND HOLD IS ASSUMED
TO BE NONINVERTING.

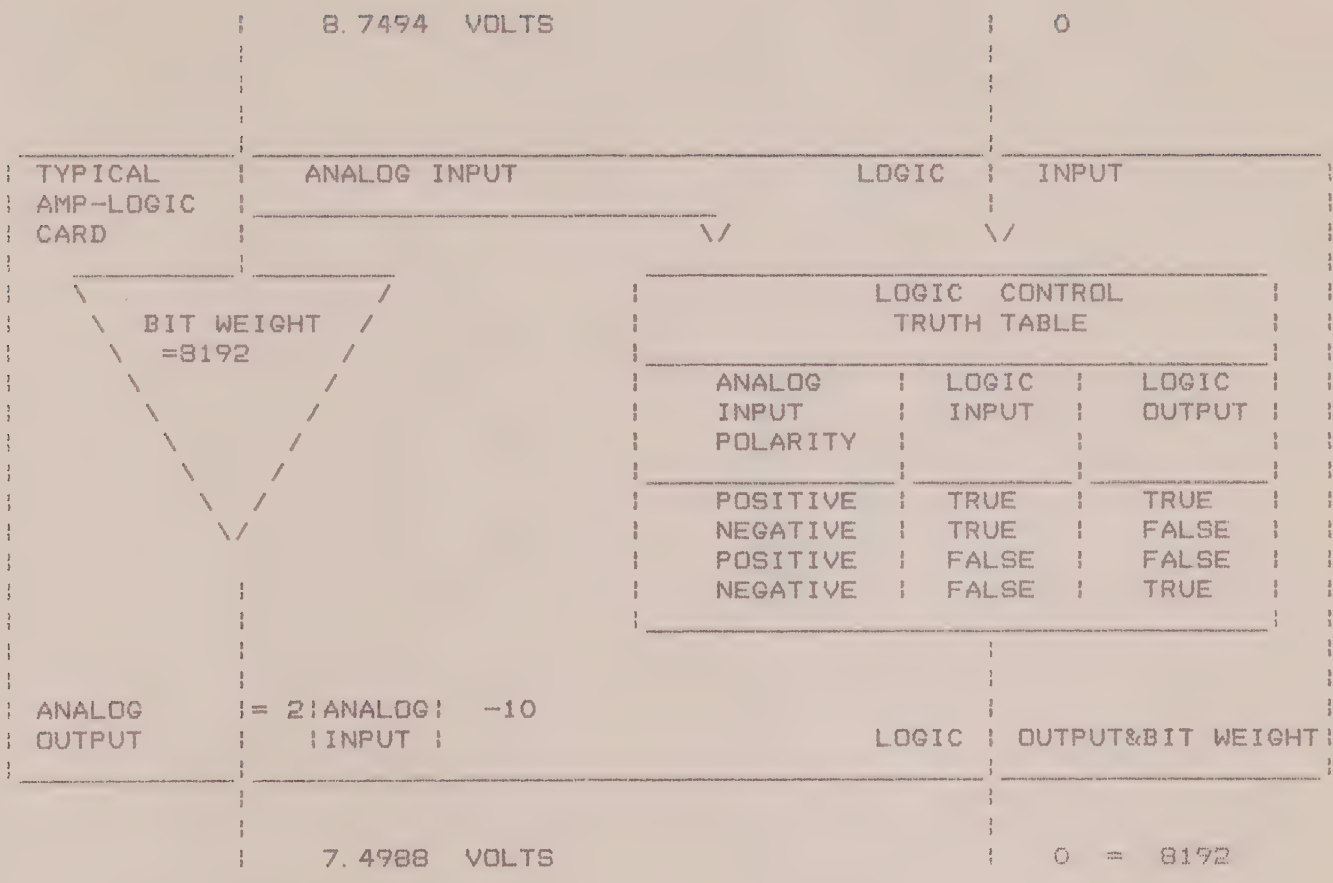


THE ABOVE DIAGRAM IS FOR BIT WEIGHT "SIGN"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)

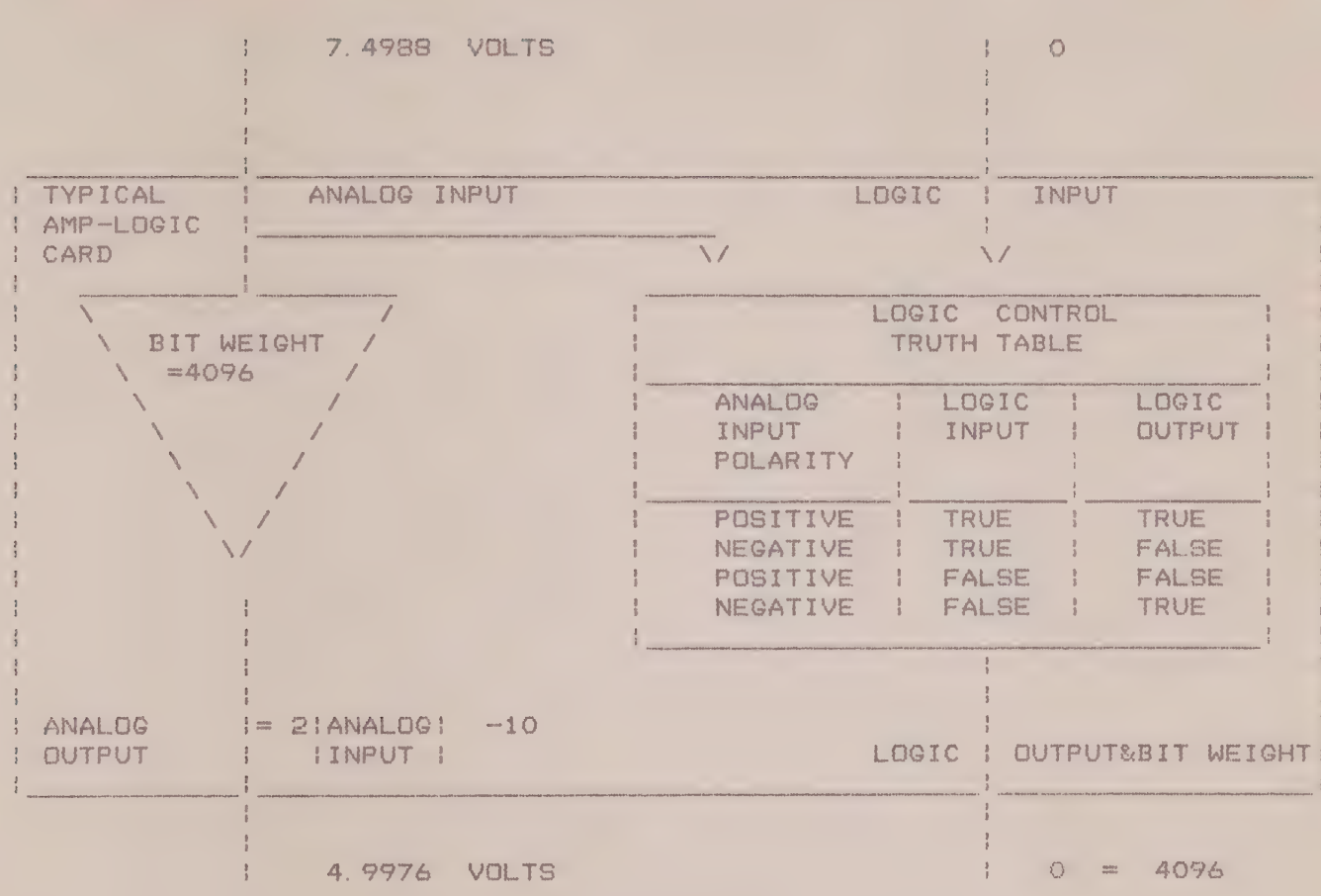


THE ABOVE DIAGRAM IS FOR BIT WEIGHT "8192"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)

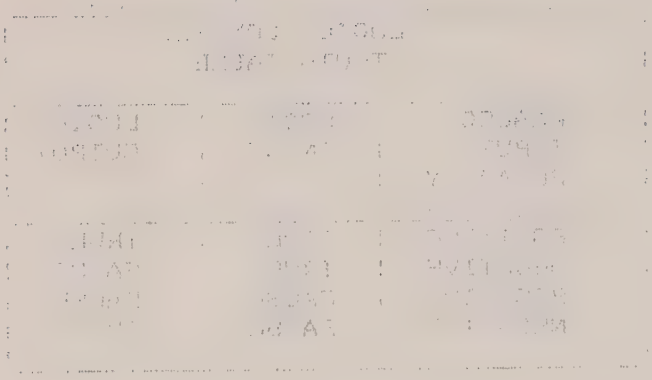


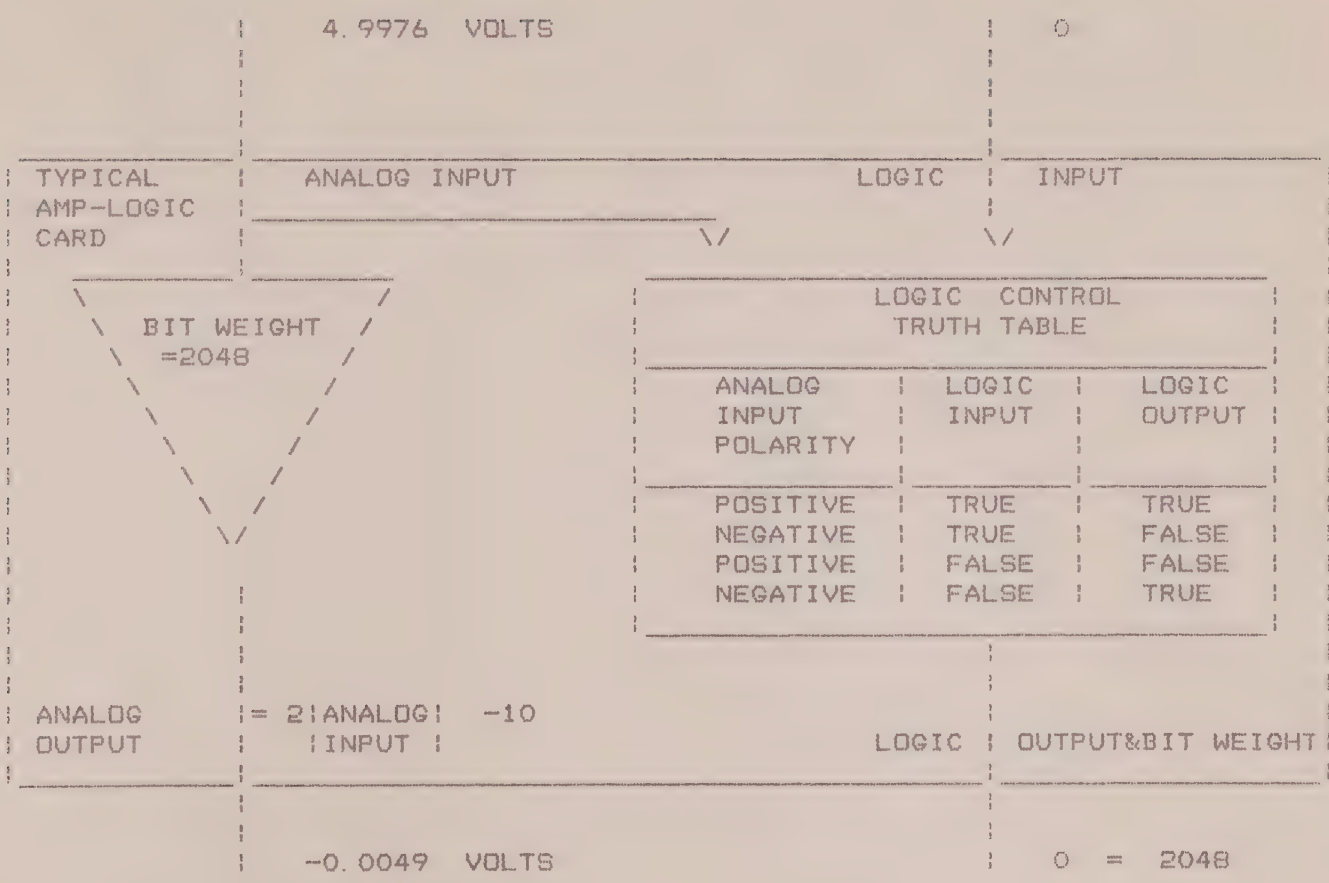
THE ABOVE DIAGRAM IS FOR BIT WEIGHT "4096"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)



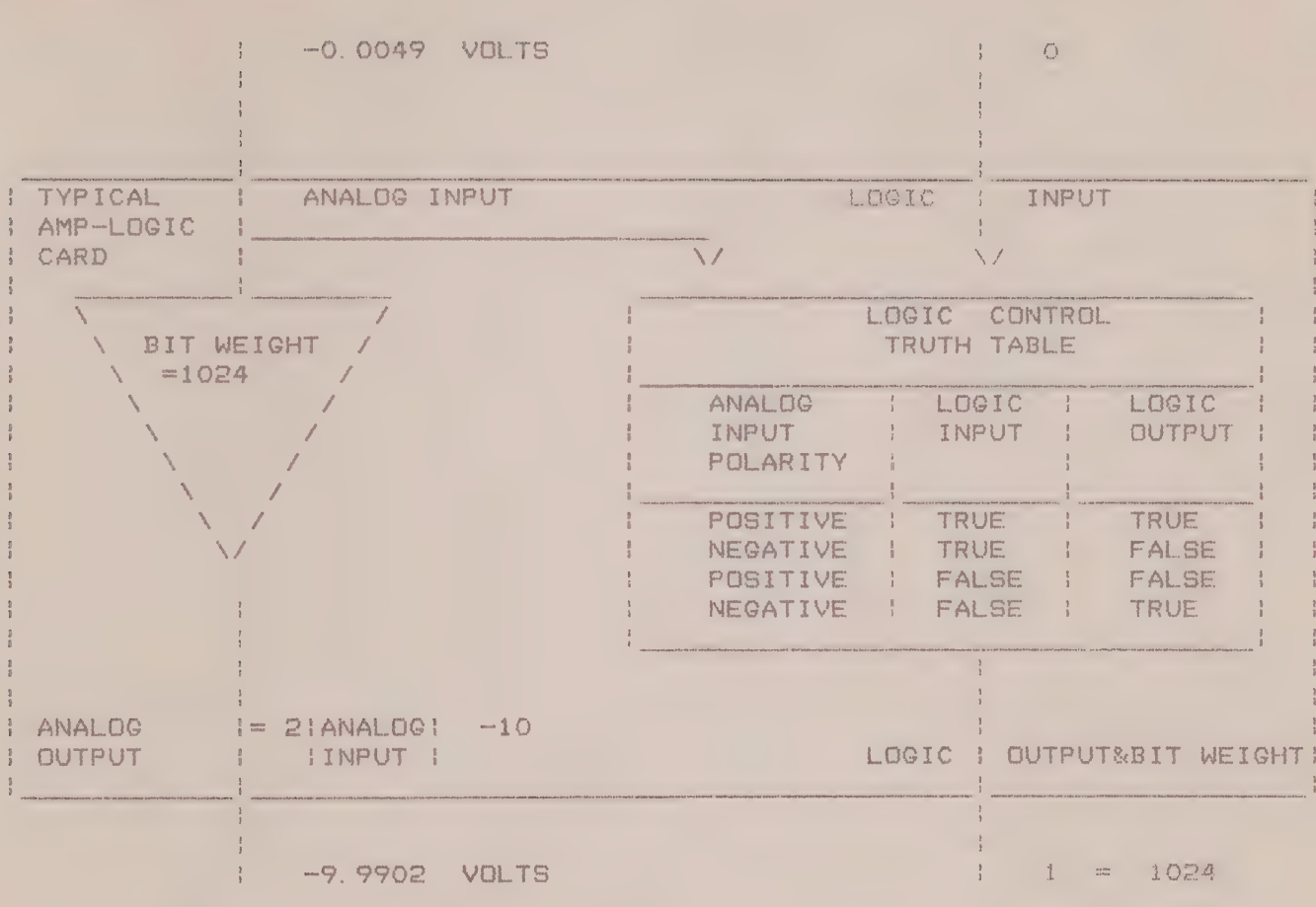


THE ABOVE DIAGRAM IS FOR BIT WEIGHT "2048"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)

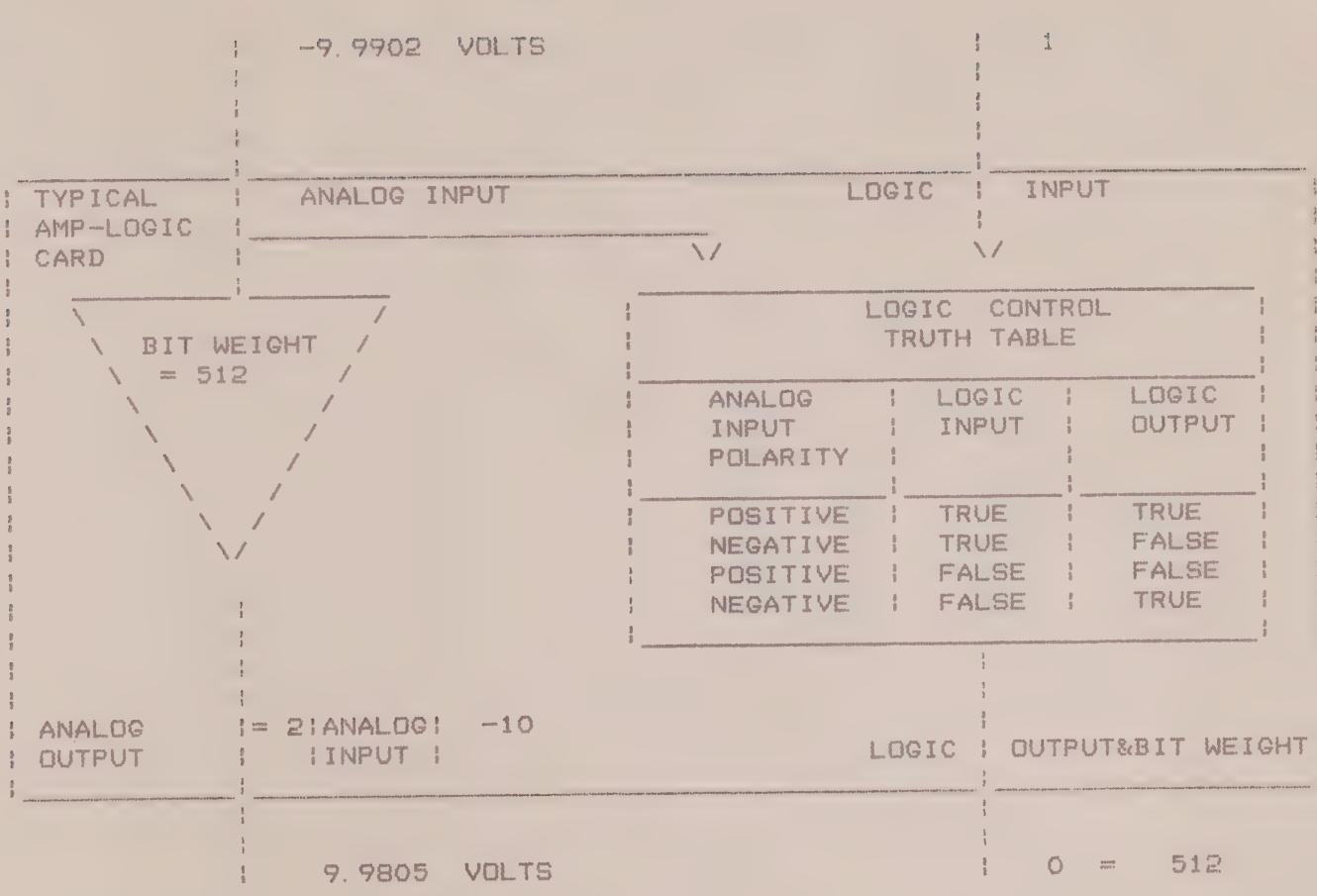


THE ABOVE DIAGRAM IS FOR BIT WEIGHT "1024"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)

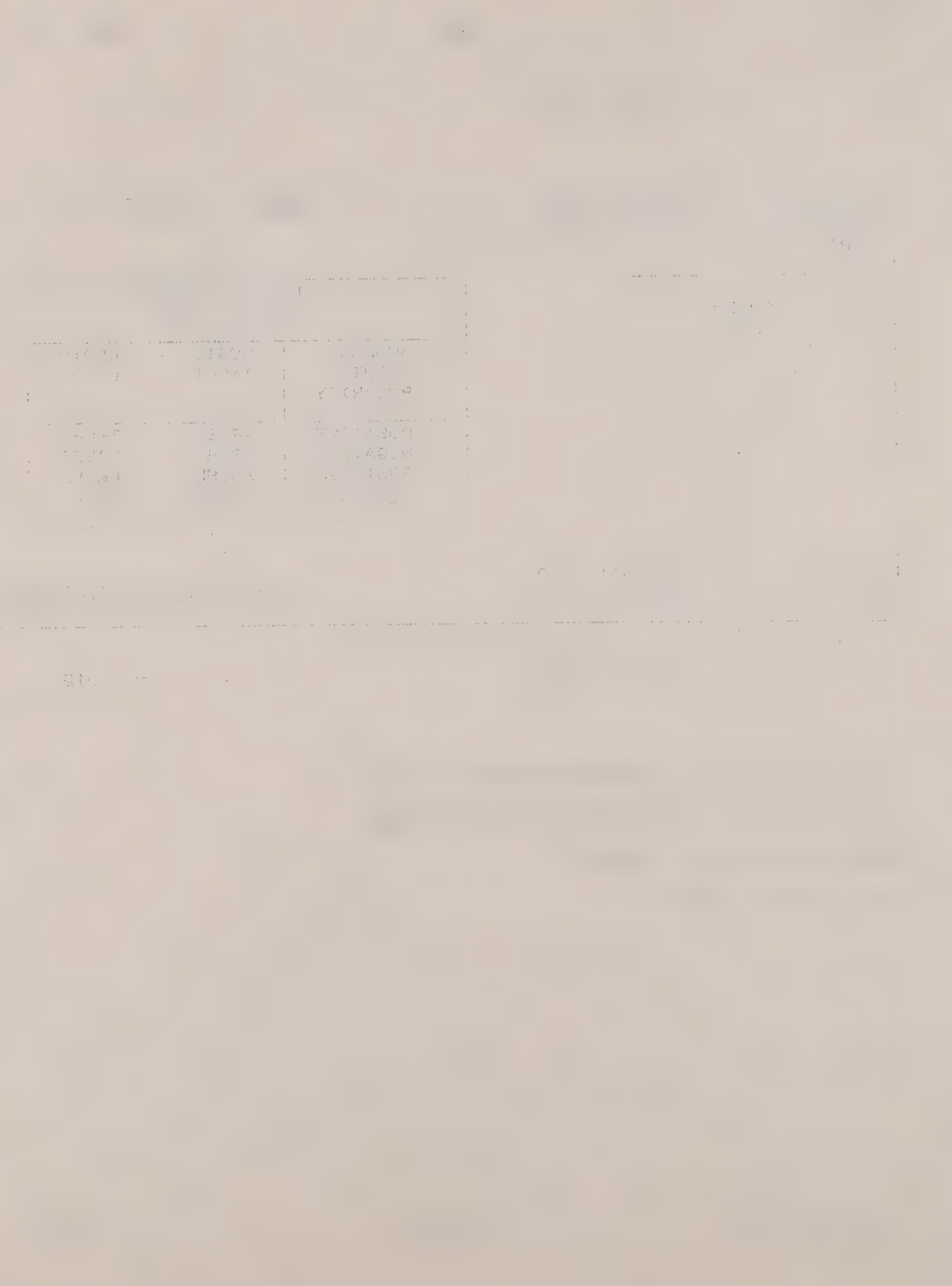


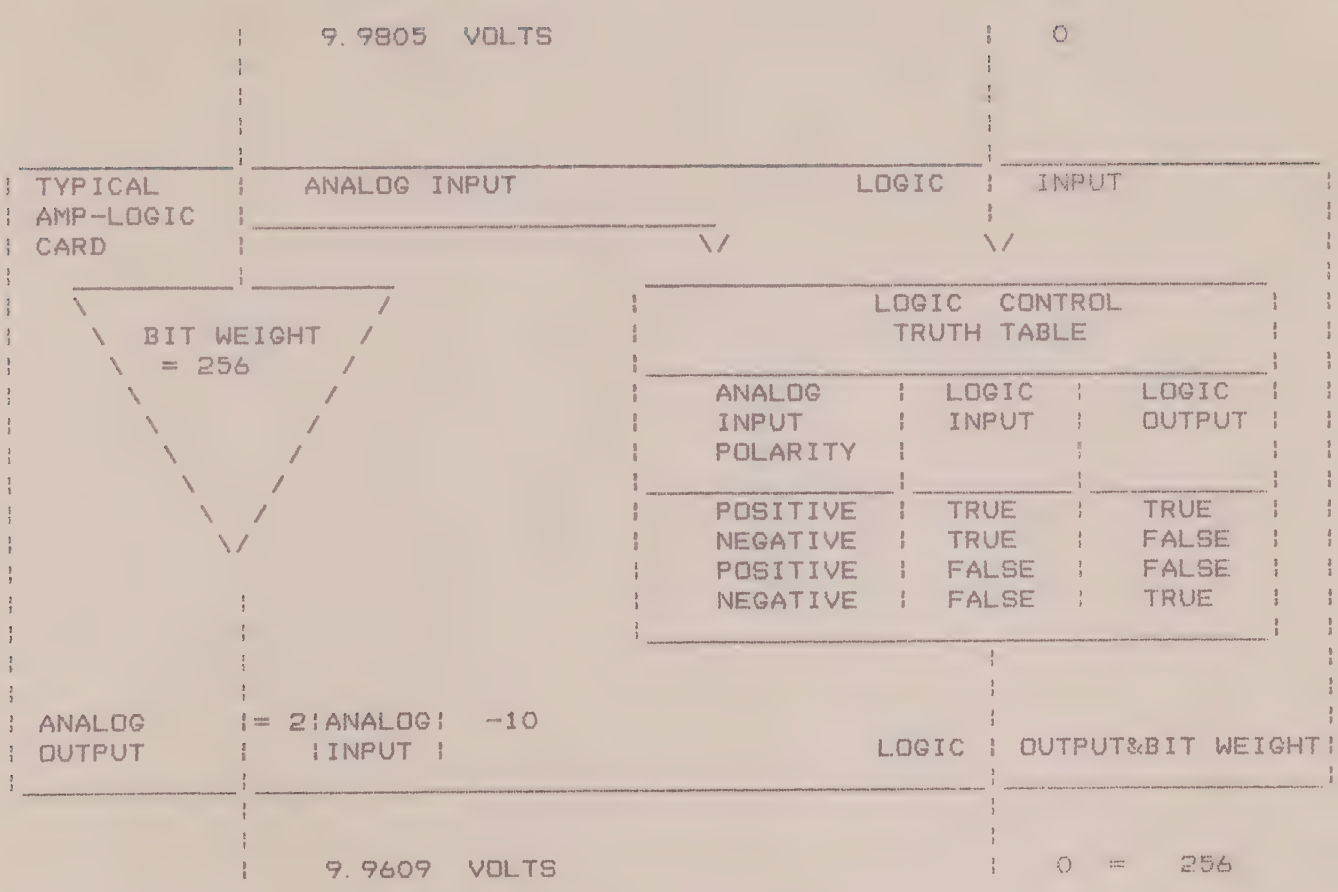
THE ABOVE DIAGRAM IS FOR BIT WEIGHT " 512"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)



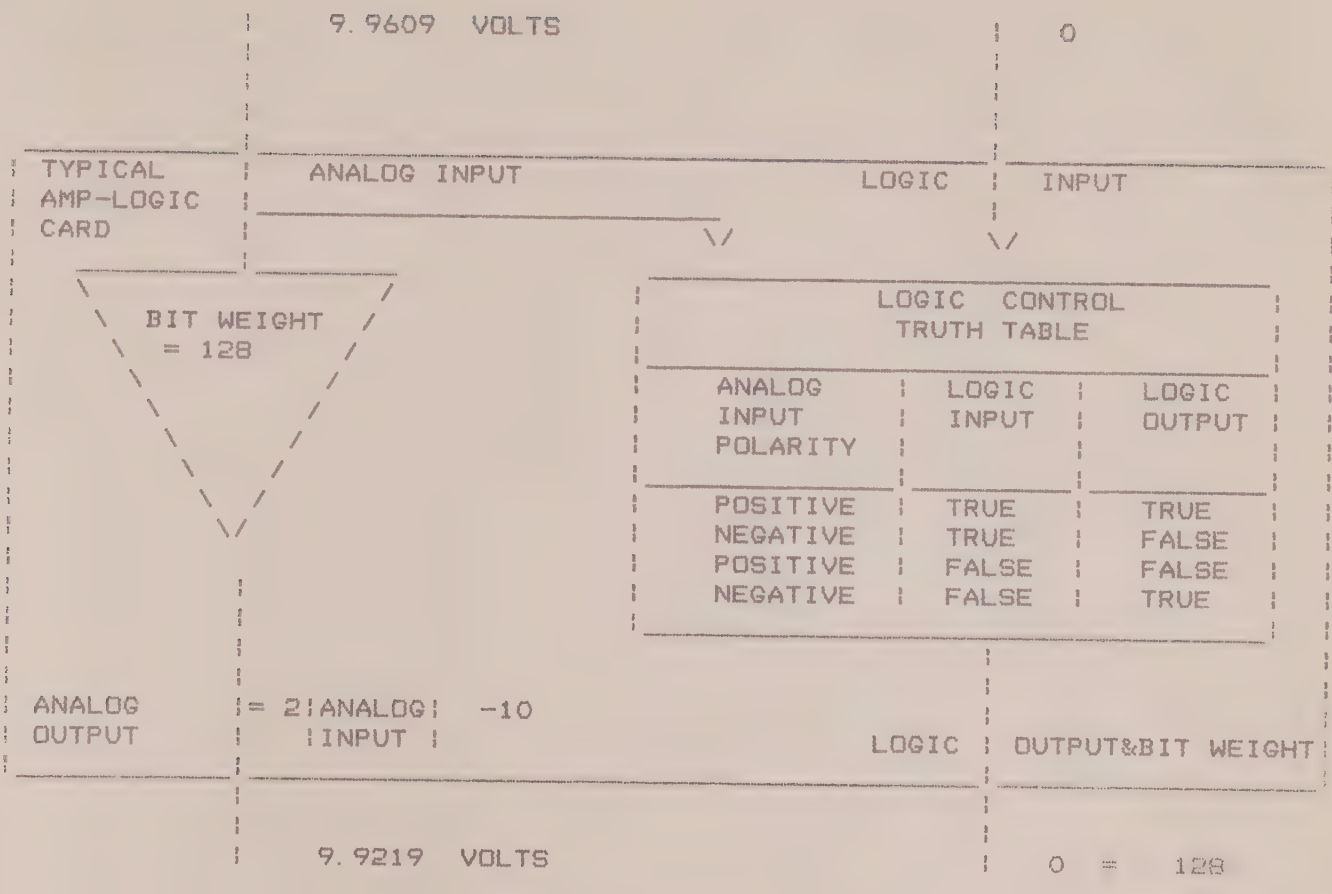


THE ABOVE DIAGRAM IS FOR BIT WEIGHT " 256"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)

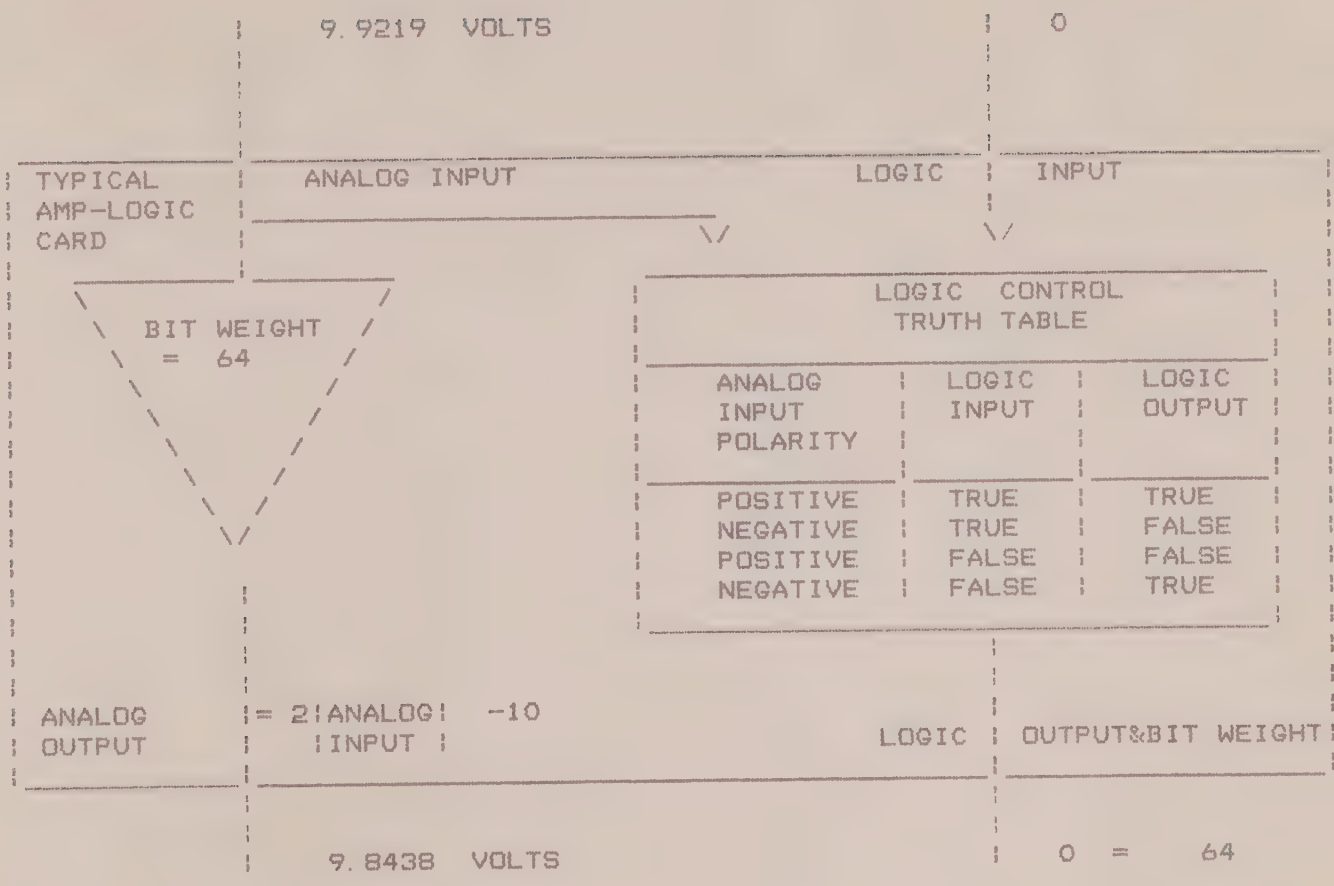


THE ABOVE DIAGRAM IS FOR BIT WEIGHT " 128"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)

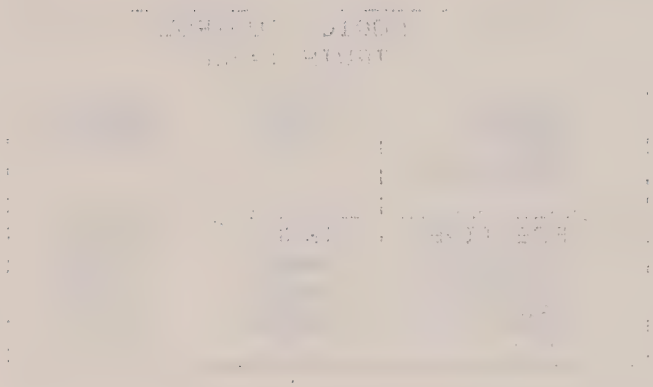


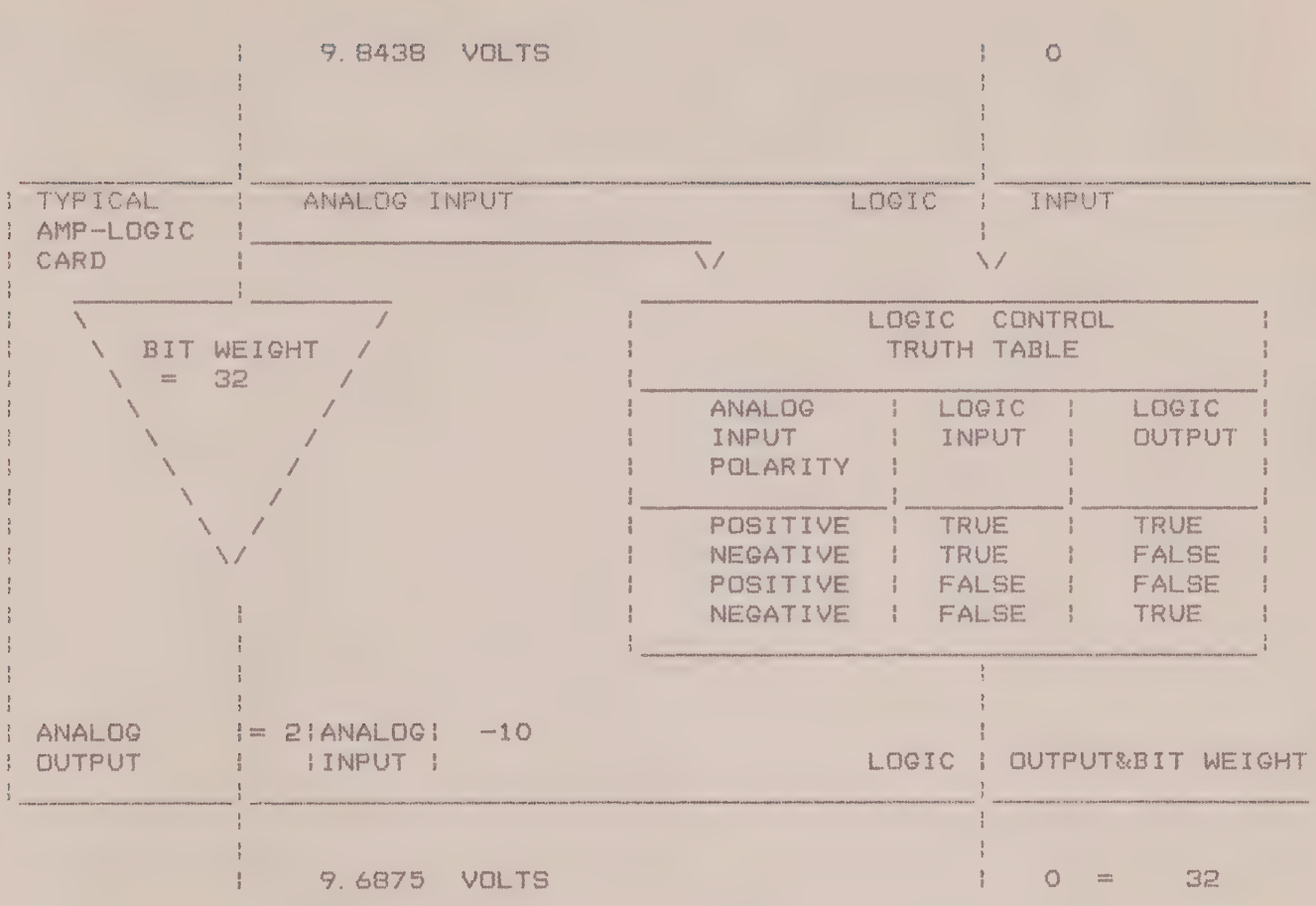
THE ABOVE DIAGRAM IS FOR BIT WEIGHT " 64"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)



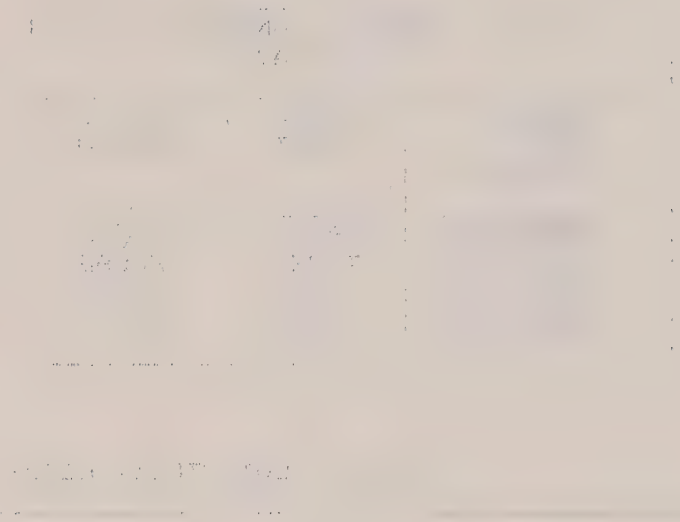


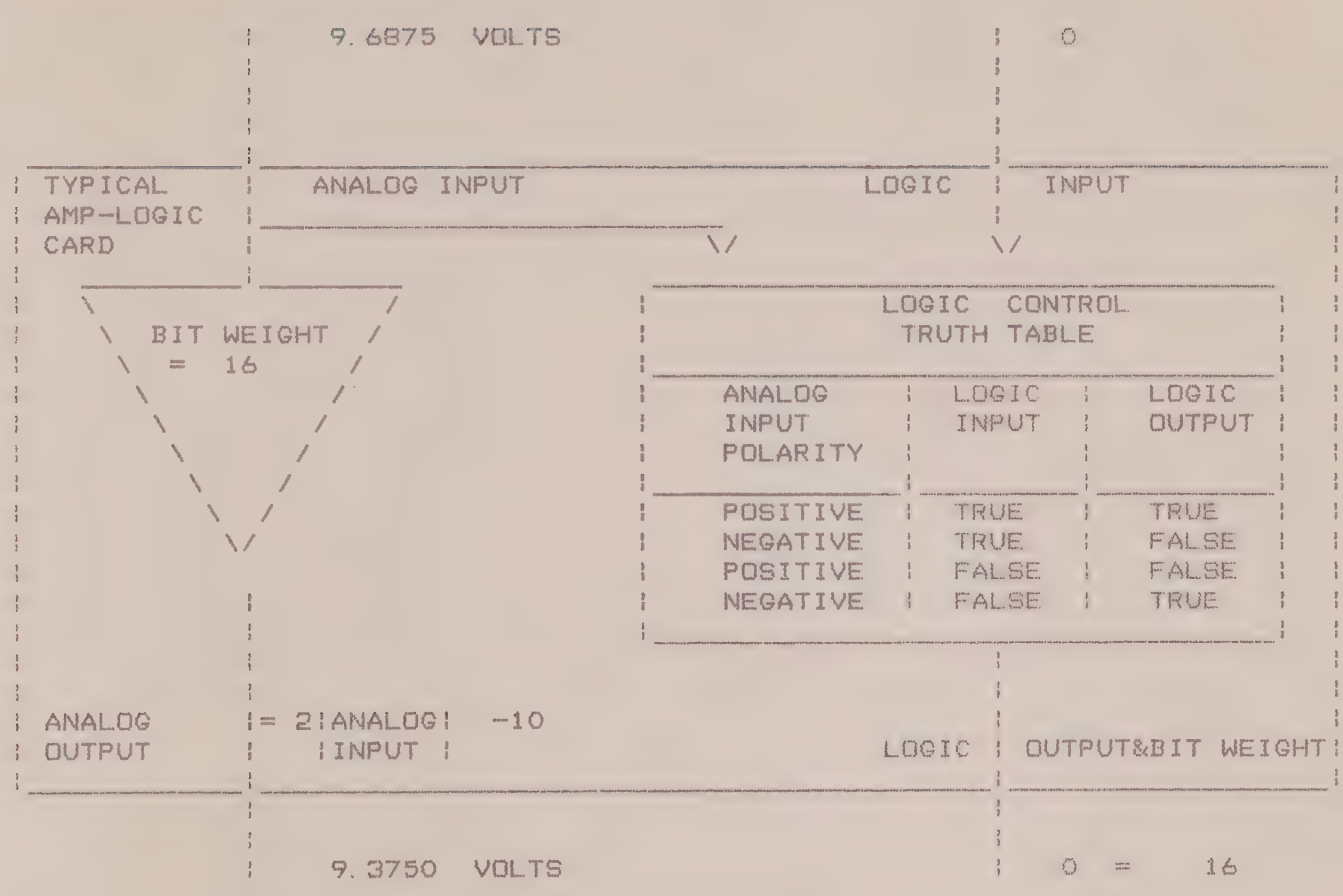
THE ABOVE DIAGRAM IS FOR BIT WEIGHT " 32"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)



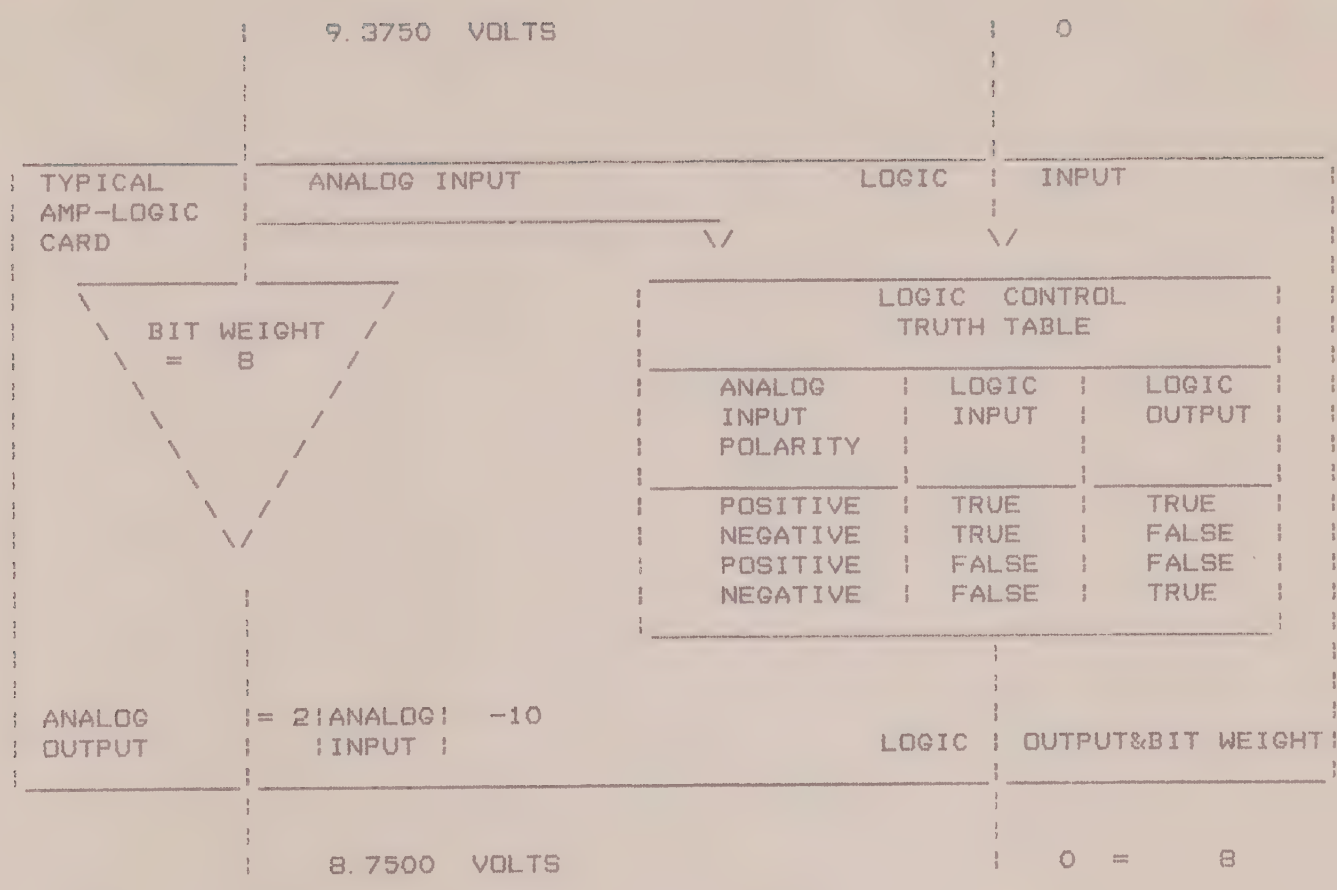


THE ABOVE DIAGRAM IS FOR BIT WEIGHT " 16"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)

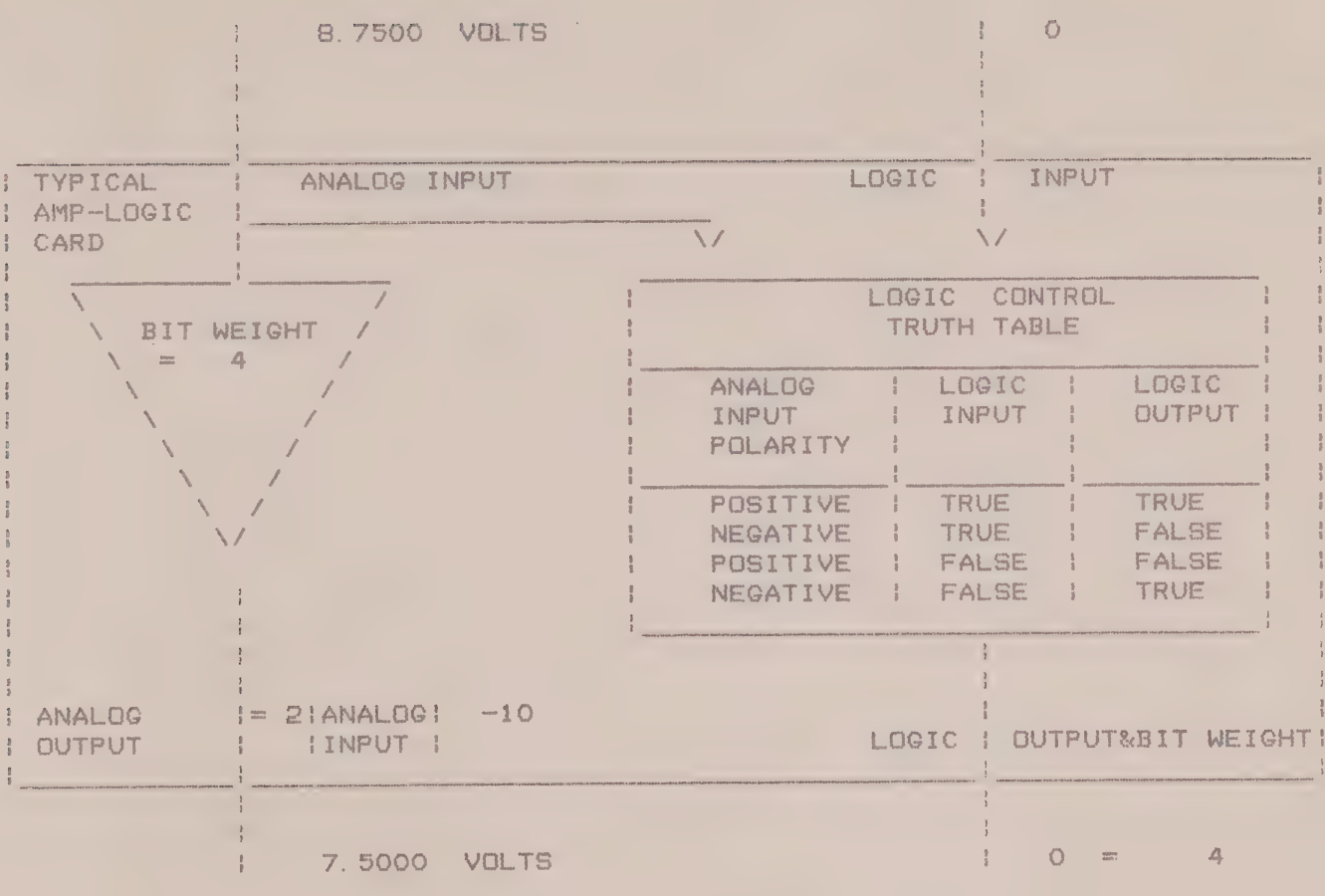


THE ABOVE DIAGRAM IS FOR BIT WEIGHT " 8"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)

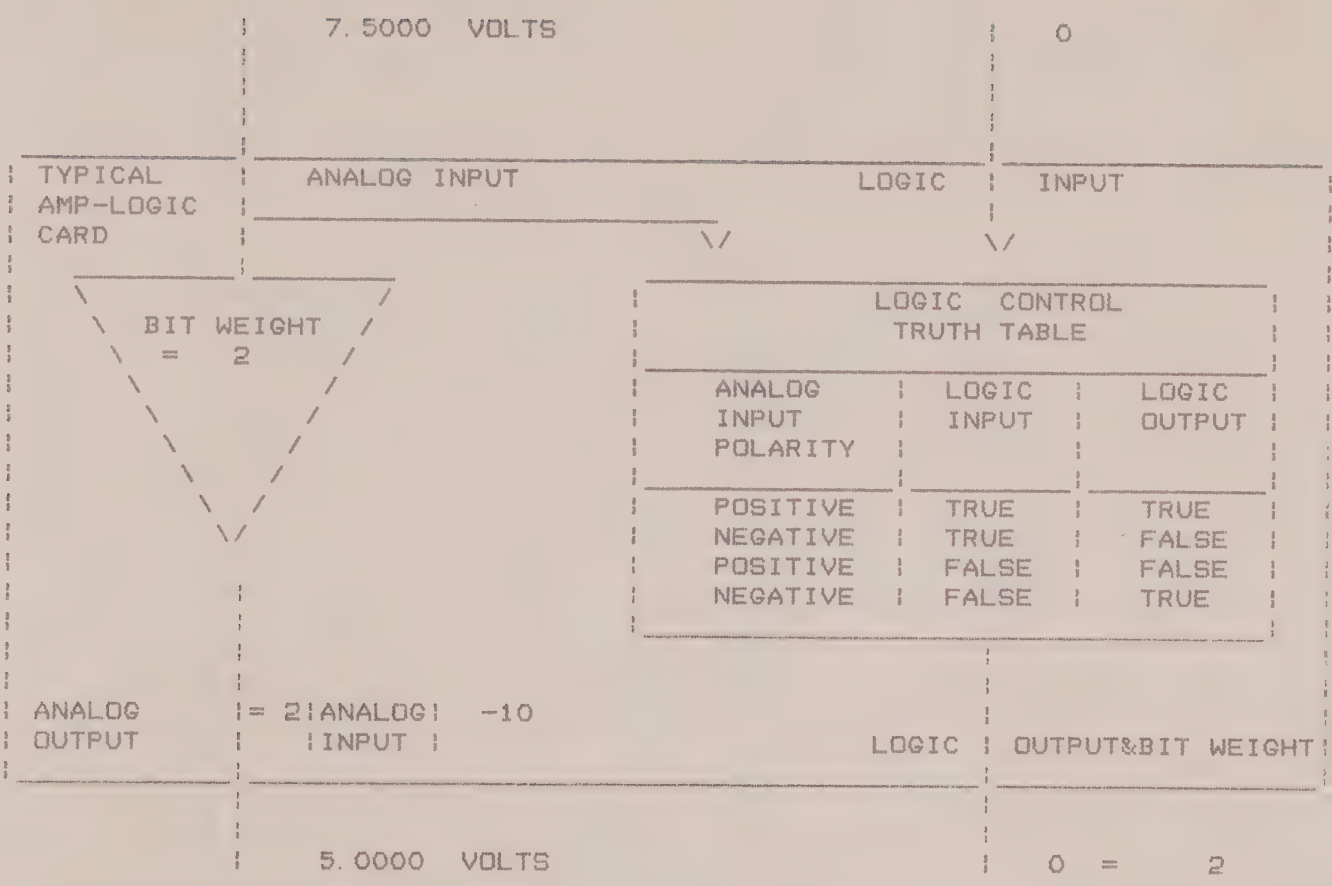


THE ABOVE DIAGRAM IS FOR BIT WEIGHT " 4"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)

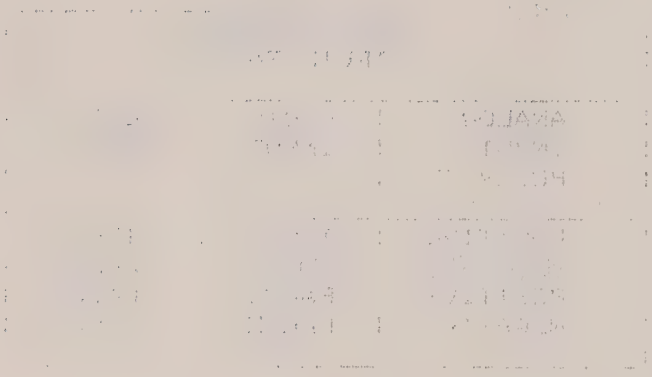


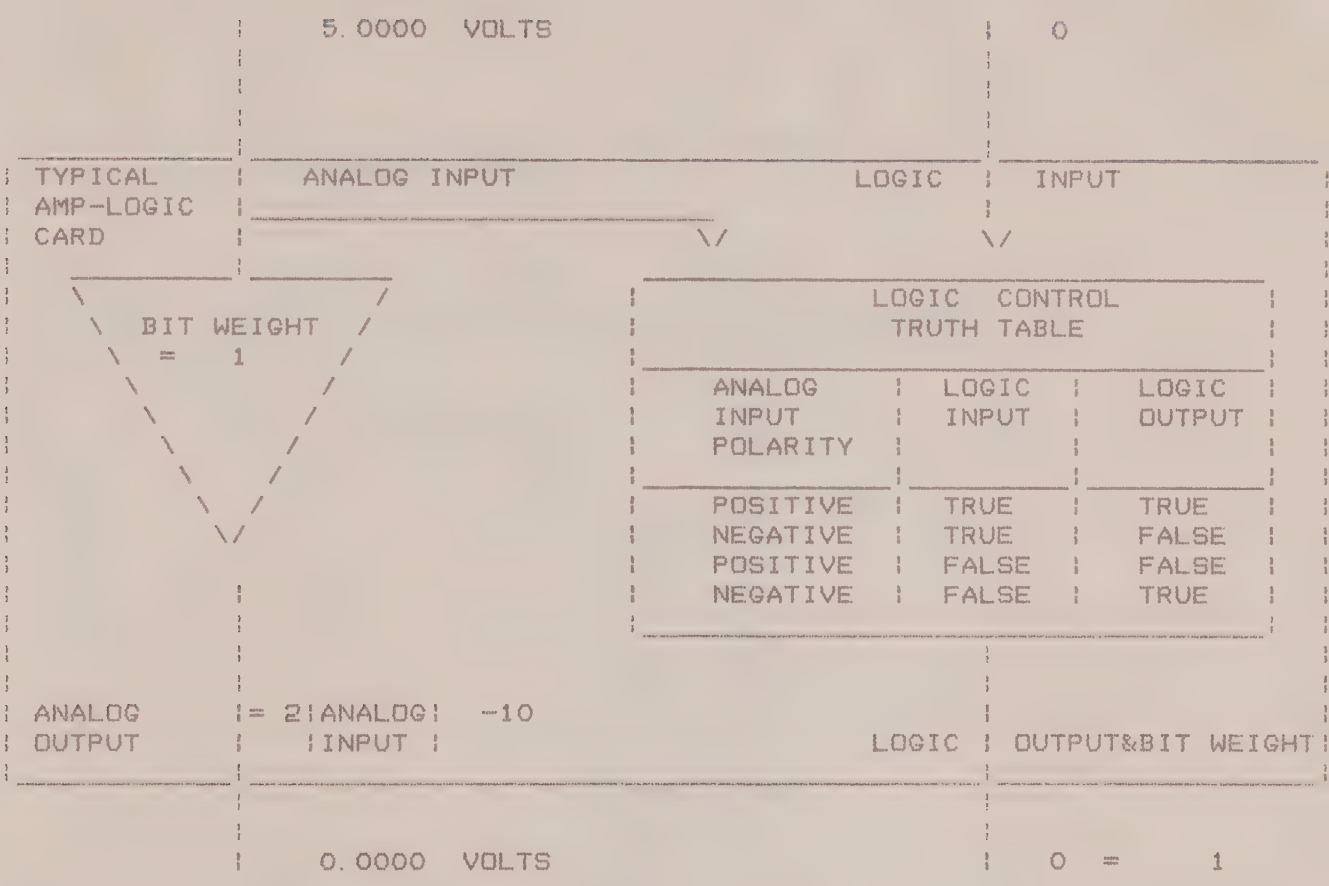
THE ABOVE DIAGRAM IS FOR BIT WEIGHT " 2"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)





THE ABOVE DIAGRAM IS FOR BIT WEIGHT " 1"

ITS ANALOG AND DIGITAL RESULTS FEED THE NEXT

AMPLIFIER AND LOGIC INPUTS.

(See the next page)

```
          !    0.0000  VOLTS                          !    0

E N D   O F   C O N V E R S I O N
THE INPUT VOLTAGE OF   -9.3750 HAS BEEN CONVERTED
INTO THE FOLLOWING BINARY DISPLAY
        0 0 0   0 1 0   0 0 0   0 0 0   0 0 0

NOTE:
THE SIGN BIT IS SHOWN AS A LOGICAL 1 FOR POSITIVE INPUTS
SINCE BOTH THE SIGN AND COMPLEMENT ARE BROUGHT OUT THE
CUSTOMER MAY USE THE COMPLEMENT FOR TWOS COMPLEMENT
OUTPUT CODES

THE OUTPUT DATA BITS ARE WEIGHTED AS FOLLOWS:
   BIT          CODE          VALUE
  SIGN           0           = NEGATIVE INPUT POLARITY
  8192           0           =   5.0000 VOLTS
  4096           0           =   2.5000 VOLTS
  2048           0           =   1.2500 VOLTS
  1024           1           =   0.0000 VOLTS
   512           0           =   0.3125 VOLTS
   256           0           =   0.1563 VOLTS
   128           0           =   0.0781 VOLTS
    64           0           =   0.0391 VOLTS
    32           0           =   0.0195 VOLTS
    16           0           =   0.0098 VOLTS
     8           0           =   0.0049 VOLTS
     4           0           =   0.0024 VOLTS
     2           0           =   0.0012 VOLTS
     1           0           =   0.0006 VOLTS

THE SUM OF THE WEIGHTS =     9.3744 VOLTS

FOR A TWOS COMPLEMENT OUTPUT CODE WITH A POSITIVE  INPUT VOLTAGE:
THE SUM OF THE WEIGHTS IS EQUAL TO THE ANALOG INPUT.

WITH A NEGATIVE INPUT VOLTAGE:  THE SUM OF THE WEIGHTS
IS EQUAL TO THE  ANALOG INPUT OFFSET BY ONE COUNT.

ONE COUNT = FULL-SCALE INPUT VOLTAGE DIVIDED BY TWO  RAISED TO THE N POWER
WHERE N IS THE NUMBER OF BITS RESOLUTION  EXCLUDING SIGN.

 FOR THIS EXAMPLE:

 FULL-SCALE      =   10.0000 VOLTS
 RESOLUTION (N)  =   14 BITS PLUS SIGN
 ONE COUNT       =    0.6104 MILLIVOLTS
 ANALOG INPUT    =   -9.3750 VOLTS
 SUM OF WEIGHTS  =    9.3744 VOLTS
```

BUFFER OR SAMPLE-AND-HOLD

When the bandwidth of the analog input signal is below approximately 100 Hz a Buffer Amplifier is normally incorporated between the multiplexer output bus and the ADC. The buffer provides a high impedance load to the output of the multiplexer. The Buffer Amplifier is available in both differential and single-ended configurations. The gain of the buffer is dependent upon the full scale of the ADC.

When wide bandwidth data is encountered, a Model GMSH Sample-and-Hold Amplifier is employed.

Figure 90016 is a block diagram of the GM Series Sample-and-Hold Amplifier. The basic design is two amplifiers in series. The first amplifier may be either differential or single-ended and provides a high input impedance with low output impedance for the Sample-and-Hold Amplifier.

The second amplifier is connected as an integrating amplifier. This amplifier follows the output of the first amplifier until the sample-and-hold command switches from the sample mode to the hold mode. When the command goes to "hold", the second amplifier is disconnected from the first amplifier and its own DC feedback and the signal that was last on the input of the integrating amplifier is held by the feedback capacitor. The DC signal can be held for as long as a millisecond before deterioration begins (see specifications Section 4).

SECTION 5

SYSTEM DESCRIPTION

INTRODUCTION

This section contains a brief general outline of your particular system. It also contains information concerning special specifications or configurations of the system.

Your GM Series Analog-to-Digital Conversion System is identified by the part number 58855-01, 58700-03, and 58845-01. This part number describes a system consisting of:

[1] One channel of Model GMD-100 AMP/MUX (channel identification No. 1).

[2] Two channels of Model GMD-1 Amplifier/Multiplexer (channel identification No's 2 and 3).

[3] Wiring for a fourth AMP/MUX identifcation No. 0.

[4] Eight (8) channels of Model GMM Multiplexer (channel identification No's 4 thru 11).

[5] Wiring for an additional eight (8) channels of GMM MUX (channel identification No's 12 thru 19).

[6] A Model GMSH-100 Sample-and-Hold Amplifier incorporated between the multiplexer bus and the input to the ADC.

[7] A Model GMAD1-15B Analog-to-Digital Converter.

[8] A Multiplexer channel expander module to increase the total channel capacity to 96 channels.

Multiplexer channel selection may be random access binary address or sequential scan via the Model GMC Logic Control System. A block diagram appears in Figure 90102.

SPECIFICATIONS

FULL SCALE: Model GMD-1 Multiplexer: +/- 10.24 volts
Model GMD-100 Multiplexer: +/- 0.1024 volts
Model GMM Multiplexer: +/- 10.24 volts

RESOLUTION: 14 binary bits and sign

OUTPUT CODE: Two's Complement

LOGIC LEVELS: Positive True TTL

OUTPUT DATA: Both the true and false sides of the data will be available at the output connector.

CONVERSION TIME: 3.5 microseconds per channel

SPECIAL FEATURE

Both the true and false sides of the sign line are made available at the rear connector. This function will allow the converter to be used as a "Zero crossing detector" in that the sign line will change as the

input signal changes polarity. A control line will be pro vided to enable function.

When the above mode is used, the Sample-and-Hold Amplifier at the A/D input should remain in the "Sample" mode. (The multiplexer cannot be dynamically operated nor the SH/AD Combination be commanded to convert when the "Zero crossing" mode is employed).

The System conforms to a Hughes Specification Number 258392 Rev. A. The first and last channel of the multiplexer may be remotely addressed.

Also this system contains both low gain and high gain Model GMD Amplifier Multiplexers.

INTERFACE CONTROL

REAR PANEL CONTROLS

MODE	F/L REG	EXT ADD	RESET	DTADC	F/L CLK	INTADC/ INTMUX CLK	MUX CLK
(1)	HI	LO	LO	GND	*	**	PULSE
(2)	X	HI	LO	GND	X	**	PULSE
(3)	LO	LO	LO	GND	X	**	PULSE
(4)	LO	LO	HI	GND	X	**	PULSE
(5)	X	X	X	PULSE	X	**	GND

(1) SEQUENTIAL EXTERNAL CONTROL
(2) RANDOM ADDRESS EXTERNAL CONTROL
(3) NORMAL MODE SEQUENTIAL FRONT PANEL CHANNEL SELECT
(4) NORMAL MODE RANDOM FRONT PANEL CHANNEL SELECT
(5) MULTIPLEXER BYPASS DIRECT TADC

X = DON'T CARE

* When operation in Mode 1 a Pulse on F/L CLK will change the First and Last channel registers, but no sequencing will occur until the MUX CLK is applied. Therefore the first and last channels may be addressed, entered and stored and then the MUX CLK may be applied when sequencing is desired.

Also if desired the F/L CLK and MUX CLK may be the same pulse or simultaneous.

** In all Modes the INT ADC and the INT MUX CLK are tied together at the rear connectors.

MODE DEFINITIONS

(1) SEQUENTIAL, EXTERNAL CONTROL

Permits sequential scan and conversion of multiplexer channels whose scan limits are set by remote first and last multiplexer address.

A channel step will be provided each time an external clock is received.

(2) RANDOM ADDRESS, EXTERNAL CONTROL

Permits signal channel selection and conversion of a multiplexer channel from a remote multiplexer address. This process is initiated by an application of an external clock.

(3) NORMAL MODE SEQUENTIAL FRONT PANEL SELECT

Permits sequential scan and conversion of multiplexer channels whose scan limits are set by the front panel first and last multiplexer address switches.

(4) NORMAL MODE RANDOM, FRONT PANEL SELECT

Permits selection and conversion of a single channel whose selection is determined by the front multiplexer address. Initiation of process requires an external clock pulse.

(5) MULTIPLEXER BYPASS, DIRECT TADC

Permits control of conversion initiation without the multiplexer delay involved. Operation requires prior selection of desired channel via the Random Modes. Upon receipt of a DTADC pulse the sample and hold amplifiers will go to the Hold MODE and a conversion will be initiated.

MULTIPLEXER EXPANDER MODULE

An Expander module P/N 58845 that will increase the total channel capacity to 96 has been designed for use with the P/N 58700 ADC System. This expander module consists of the following multiplexer models.

MODEL	DESCRIPTION	CHANNEL NUMBER
GMD-10	FS=+/-1.024 volts	20-29
GMD-0.75	FS=+/13.6533 volts	30-31
GMD-0.5	FS=+/-20.48 volts	32-39
GMD-0.25	FS=+/-40.96 volts	40-51
GMD-0.125	FS=+/-81.92 volts	52-55
GMMD	FS=+/-10.24 volts	64-103

Multiplexer channel control is via the Model GMC Logic Control System mounted in the P/N 58700 Card Module.

ANALOG OUTPUTS

The continuous analog output from the Model Gmd Channels 20, 21, 32, 33, 40, 41, 52, and 53 is available on one multipin Wichester connector.

SECTION 6

CALIBRATION

INTRODUCTION

This calibration procedure describes the step-by-step method for calibrating the GM Series Multiplexing Analog-to-Digital Conversion System. Hardware and placement of certain boards may be different depending upon each customer's requirement, but basic calibration is the same for each individual instrument.

Please refer to the top assembly drawing for the individual plug-in-board placement. Refer to the assembly drawings of each individual plug-in board for variable resistor and capacitor placement, pin numbers, and test points. All of the above are located in Section 11.

When making adjustments in the preliminary and final calibration, it will be necessary to maintain a proper air flow within the chassis. For the preliminary calibration, remove the top cover, turn it over and place it on top of the unit so that only the first row of boards will

be visible. This will maintain near proper air flow and still allow access to the ADC calibration and timing adjustmments that will be made during the preliminary calibration.

During the final calibration, the unit will most likely be in an environmental chamber. The top and bottom covers should be in place during the measurements. If an adjustment is necessary, the cover can be removed for these adjustments. However it is recomended that the adjustment be made in the shortest time possible and the cover be replaced after the adjustment is made. After the cover has been replaced, time should be allowed for the air flow to return to normal before recording any further measurements.

Your A/D Converter System has undergone complete calibration in our factory test department (a copy of the original test report is provided in Section 12 of this document). Assuming there are no catastrophic failures, it should not be necessary to perform a detailed calibration on this equipment for several years. It will be necessary to periodically verify the calibration (using the following procedure). The recommended time between calibration verification is six months. Before any attempt to calibrate the instrument is made, a check should be performed to verify that the unit is either in or out of specification and does indeed need calibration.

(a) Refer to the factory test report for a review of the full scale, output, binary code, resolution, etc.

(b) Select the digital output binary values that are of or near 1/2, 1/4, 1/8 or 1/16 full scale in both polarities (refer to the test report for examples of these numbers).

(c) Introduce the analog value into the ADC to produce one of the binary numbers mentioned in Step (b).

(d) By comparing the readings derived in Step (c) with known correct numbers, it can be determined if the unit is in or out of specification and whether calibration of the unit is necessary.

The results can also be compared to the factory test report results if the binary values listed on the report were used in Step (b). If the factory test results are used as a guide in determining the binary values to be checked, there may be a difference between the value shown on the test report and your results. Although this difference may occur, the value to rely on for determining the validity of the calibration will be the difference between your results and the theoretical input value. The error margin is noted at the top of the test report and is nomenclatured as "THEORETICAL ANALOG INPUT +/-____millivolts".

TEST EQUIPMENT

Equipment recommended for calibration consists of the following:

(a) A stable DC analog voltage source, variable over the range of +/- full scale input voltage or +/-10 volts whichever is greater. The voltage resolution should be at least 25% of the least significant bit. The source impedance should be less than 1000 ohms.

(b) Oscilloscope, Tektronix 545A, with 1A5 and CA Preamplifiers, or equivalent.

(c) Five-digit digital voltmeter, differential voltmeter, or equivalent. The accuracy should be at least twice that of the system being tested.

(d) Triangle wave generator with a capability of 20 volts peak-to-peak into a 470 ohm load at 1 kHz.

(e) VOM such as Simpson 260.

(f) Pulse generator to provide clock pulses of an equivalent in amplitude width and frequency to the normal system operating pulses.

(g) Printed circuit card extender, bit board extender (Part No. 52315) and Sample-and-Hold Buffer extender (Part No. 52318). All three are supplied with the unit. (Part No. 52315 and 52318 may be replaced by

a single extender Part No. 52330.)

PRELIMINARY CALIBRATION (at room temperature 25 +/-3C)

In the GM Series ADC each binary bit is controlled by a single printed circuit board with the exception of the four least significant bits. During calibration, each board will be adjusted individually starting with the least significant bit (excluding 1, 2, 4 and 8). There are some adjustments that relate to the least four bits and the adjustments are discussed in this section.

(a) Check the plus and minus reference supplies and set them for 10.000 volts.

(b) Locate the least significant bit board (excluding the least four bits 1, 2, 4 and 8). This will be the AMP/Logic board nearest to 4 bit amplifier board. (Normally bits 1, 2, 4 and 8 are on two boards and are not adjusted per this procedure). If the ADC does not contain a four bit amplifier and a four bit logic board disregard the references to these boards and begin the procedure with the least significant bit board.

(c) Remove the next more significant AMP/Logic Board located just prior to the one mentioned in Step (b) and replace it with the Bit Board Extender.

(d) This board is designed to allow the operator to isolate a

particular board from the higher order bits and introduce an input directly into that bit board. The operator may use a standard extender board and use the following pin numbers for connecting the input signal.

BIT BOARD EXTENDER	LABEL
Pin #9	Input Hi
Pin #4 and #5	Ground (low)

NOTE: JUMPER PINS 38 TO 35 (logic).

For extender replacement of the Sample-and-Hold board, the pin numbers are as follows:

SAMPLE-AND-HOLD

EXTENDER	LABEL
Pin #22	Input Hi
Pin #16	Input Low (Gnd.)

NOTE: DO NOT JUMPER PIN 38 TO 35 AS ABOVE.

(e) Connect the DVM through a 470 ohm resistor to the test points marked A2 and ANA GRD (Figure 90017) located on the least significant

bit board, (excluding the 4 bit amp and logic boards). This is normally the last "C" board. Connect the variable DC source (with monitor) to the signal board extender (Pins 4 and 9). The input value must be measured directly at Pins 4 and 9 or remote sense lines must be used to compensate for the voltage drop in the input cable.

(f) Set the DC source for minus 10 millivolts and note the reading of the DVM.

(g) Set the variable DC source for plus 10 millivolts and adjust potentiometer label B0 so that a plus 10 millivolt input produces the same reading (at A2) as minus 10 millivolts did. Switch between plus 10 millivolts and minus 10 millivolts and adjust B0 with the plus 10 millivolts input until there is no change in the reading of the DVM.

(h) Set the variable DC source for 0 VDC and adjust the potentiometer labeled zero until the reading at A2 is as close as possible to minus 10 volts.

(i) Set the variable DC source for plus 10 volts and adjust the potentiometer S2 for a plus 10.000 volt reading at test point A2 (Figure 90017).

(j) Set the variable DC source for minus 10 volts and adjust potentiometer S1 for a plus 10.000 volt reading at test point A2 (Figure 90017).

(k) Repeat paragraph number two of step (f) and (g) to check the symmetry.

(l) Repeat step (h) to check the zero setting.

(m) Repeat step (i) and (j) to check the full scale of the bit board.

(n) Return voltage input to 0 volts.

SUBSEQUENT BIT BOARD ADJUSTMENT

(a) Remove the signal board extender.

(b) Replace the bit board that had been previously removed.

(c) Remove the next more significant bit board and insert the signal board extender.

(d) Set the DC source for minus 10 millivolts and note the reading of the DVM.

(e) Set the variable DC source for plus 10 millivolts and adjust potentiometer label B0 so that a plus 10 millivolt input produces the same reading (at A2) as minus 10 millivolts did. Switch between plus 10 millivolts and minus 10 millivolts and adjust B0 with the plus 10 millivolts input until there is no change in the reading of the DVM.

(f) Set the variable DC source for 0 VDC and adjust the potentiometer labeled zero until the reading at A2 is as close as possible to minus 10 volts.

(g) Set the variable DC source for plus 10 volts and adjust the potentiometer S2 for a plus 10.000 volt reading at test point A2 (Figure 90017).

(h) Set the variable DC source for minus 10 volts and adjust potentiometer S1 for a plus 10.000 volt reading at test point A2 (Figure 90017).

(i) Repeat paragraph number two of step (f) and (g) to check the symmetry.

(j) Repeat step (h) to check the zero setting.

(k) Repeat step (i) and (j) to check the full scale of the bit board.

(l) Return voltage input to 0 volts.

(m) Repeat steps (a) through (n) for all bit boards in sequence moving from the least significant "C" board through the most significant "B" board.

(n) Perform the calibration steps as outlined in "FOUR BIT CALIBRATION" for the 4 bit amplifier/logic boards.

(o) Repeat steps (a) through (c) for the "AB" amplogic board.

NOTE: From this point on in the calibration procedure, the front panel digital readout lamps will be used to monitor the results of the adjustments.

(p) Set the input to the AB board for minus 0.078 volts. Adjust the zero potentiometer on the "AB" board, refer to Figure 90017, for a digital readout of X X X X X 1 0 0 0 0 0 0 ____* (ignore the readouts represented by the X).

*The 3 least significant bits are used for the transition point recognition. The transition point is the point where the 3 to 4 binary change takes place. The lights will appear to be only partially ON and this should not be confused with the binary number 7 where all indicators are ON full.

(q) Set the input to the "AB" board for a plus 0.078 volts. Adjust the B0 potentiometer on the "AB" board for a digital readout of:

X X X X X 0 1 1 1 1 1 1 _____*

(r) Set the input to the "AB" board for minus 9.922 volts and adjust the S1 potentiometer for a digital readout of:

X X X X X 1 1 1 1 1 1 1 ____*

(s) Set the input to the "AB" board for plus 9.922 volts and adjust the S2 potentiometer for a digital output of:

X X X X X 0 0 0 0 0 0 0 ____*

(t) Repeat steps (a) through (c).

(u) Set the input to the 'A' analogic board (Figure 90018) for plus 0.117 volts and adjust the Z1 potentiometer for a digital output of:

X X X X 0 1 1 1 1 1 1 0 ____*

(v) Set the input for minus 0.195 volts and adjust the Z2 potentiometer for a digital output of:

X X X X 1 0 0 0 0 0 1 0 ____*

(w) Set the input for plus 9.805 volts and adjust the K1 potentiometer for a digital output of:

X X X X 0 0 0 0 0 0 1 0 ____*

(x) Set the input for minus 9.883 volts and adjust the K2 potentiometer for a digital output of:

X X X X 1 1 1 1 1 1 1 0 ____*

(y) Repeat steps (a) through (c).

(z) Repeat the steps (u) through (x) using the following input voltages and adjusting the respective potentiometers for the indicated digital outputs.

INPUT	ADJUST	DIGITAL OUTPUT
+ 0.0586	Z1	X X X 0 1 1 1 1 1 1 1 0 ____*
- 0.0976	Z2	X X X 1 0 0 0 0 0 0 1 0 ____*
+ 9.9023	K1	X X X 0 0 0 0 0 0 0 1 0 ____*
- 9.9415	K2	X X X 1 1 1 1 1 1 1 1 0 ____*

(aa) Repeat steps (a) through (c).

(ab) Repeat steps (u) through (x) using the following input voltages and adjust the respective potentiometers for the indicated digital outputs.

INPUT	ADJUST	DIGITAL OUTPUT
+ 0.0293	Z1	X X 0 1 1 1 1 1 1 1 1 0 ____*
- 0.0488	Z2	X X 1 0 0 0 0 0 0 0 1 0 ____*
+ 9.9512	K1	X X 0 0 0 0 0 0 0 0 1 0 ____*
- 9.9707	K2	X X 1 1 1 1 1 1 1 1 1 0 ____*

(ac) Repeat steps (a) through (c).

(ad) Repeat steps (u) through (x) using the following input voltages and adjust the respective potentiometers for the indicated digital outputs.

INPUT	ADJUST	DIGITAL OUTPUT
+ 0.0147	Z1	X 0 1 1 1 1 1 1 1 1 1 0 _____*
- 0.0244	Z2	X 1 0 0 0 0 0 0 0 0 0 1 0 _____*
+ 9.9756	K1	X 0 0 0 0 0 0 0 0 0 0 1 0 _____*
- 9.9854	K2	X 1 1 1 1 1 1 1 1 1 1 1 0 _____*

(ae) Repeat steps (a) through (c)

(af) Repeat steps (u) through (x) using the following input voltages and adjust the repective potentiometers for the indicated digital outputs.

INPUT	ADJUST	DIGITAL OUTPUT
+ 0.0122	Z1	0 1 1 1 1 1 1 1 1 1 1 0 _____*
- 0.0078	Z2	1 0 0 0 0 0 0 0 0 0 1 0 _____*
+ 9.9924	K1	0 0 0 0 0 0 0 0 0 0 1 0 _____*
- 9.9881	K2	1 1 1 1 1 1 1 1 1 1 1 0 _____*

(ag) At this point the buffer on Sample-and-Hold Amplifier may be installed and the ADC checked for final calibration, continue with the Buffer Amplifier portion of this section.

FOUR BIT CALIBRATION (Figure 90020)

(a) Remove the bit board preceding the 4 bit amp.

(b) Place the board extender into the slot.

(c) Connect a triangular wave generator to the signal board extender inputs.

(d) Set the output of the generator for triangular wave of 20.0 volts peak-to-peak 1 kHz (symmetrical about zero + 10V.0V to - 10V.0V)

(e) View the output AMP 1 on an oscilloscope and set the symmetry BO 1 so that all waves on the scope are symmetrical about the triangle peaks.

(f) Set the potentiometer Z1 so that the output is symmetrical about zero.

(g) Repeat steps (e) and (f) for amplifier output AMP 2 using BO2 and Z2 potentiometers.

(h) View the test point for AMP 3 and adjust BO 3 and BO 4 so that there is less than 10% phase modulation of the displayed square wave over one cycle of sawtooth wave.

FOUR BIT CALIBRATION (alternate method)

(a) Do steps (a) and (b) of the previous Four Bit Calibration procedure and center all potentiometers.

(b) Connect a precision DC source to the signal board inputs.

(c) Set the input to 0 volts and adjust the B01 potentiometer so that the front panel least significant bits toggle between 0 1 1 1 and 1 0 0 0.

(d) Change the input to plus 2.5 volts and adjust B03 potentiometer so that the front panel display toggles between 0 1 0 1 and 0 1 1 0.

(e) Change the input to plus 1.25 volts and adjust B04 so that the front panel display toggles between 0 1 1 0 and 0 1 1 1.

(f) Change the input to plus 5 volts and adjust B02 potentiometer so that the front panel display toggles between 0 0 1 1 and 0 1 0 0.

(g) Check steps (c) and (f).

(h) Change the input to plus 8.75 volts and adjust Z1 potentiometer so that the front panel display toggles between 0 0 0 0 and 0 0 0 1.

(i) Run a linearity check per Figure 90019.

(j) The total error should not exceed +/-0.25 volts.

CLAMP ADJUSTMENT (LOGIC "A" BOARDS)

The folowing procedure has been done during factory calibration. It is not necessary to perform this procedure unless a component connected with the CLAMP circuit hs been replaced.

PROCEDURE

(a) Set up for the monotinicity test as described in Figure 90114 and Figure 90120.

(b) Adjust the triangle generator to obtain a pattern as shown in Figure 90119(1).

(c) Adjust the DC source to obtain a pattern as shown in Figure 90119(2). At this point you should have a display as described by the entire Figure 90119. The portion of the figure that will be of interest will be the center (longest string of steps). This will be the part of the display that contains the bit in question (the bit in question being the bit output from the board under test).

(c) Turn the potentiometers CP1 and CP2 full clockwise.

(d) Turn the potentiometer CP1 counter-clockwise until the BIT disappears from the center of the displayed pattern.

(e) Turn the potentiometer CP1 clockwise 2 turns.

(f) Repeat the above steps for potentiometer CP2.

BUFFER AMPLIFIER

PRELIMINARY

All GM Analog-to-Digital Converters will have either a Sample-and-Hold or a Buffer Amplifier at the input to the ADC.

The calibration of the Buffer Amplifier should be done after the calibration of the ADC bit boards in order to allow the ADC to be used as a measuring instrument.

If there is not a multiplexer involved in the same chassis as the ADC, direct connection to the input of the buffer can be accomplished at the rear panel connector.

If a multiplexer is involved in the ADC chassis, connection to the input of the buffer may be accomplished by either of two methods:

(a) Selection and addressing of a particular multiplexer channel and removal of the board containing that channel to enable connection to the input of the buffer through the common bus line of the multiplexer using the extender board.

(b) Selection and addressing of a particular multiplexer channel and removal of the board containing that channel and then placing the Buffer Amplifier on an extender board and connecting to the input of the buffer directly through pins of the Buffer Amplifier itself.

COMMON MODE RTO (Refer to Figure 90021)

The common mode adjustment need only be made if the Buffer Amplifier is to be used as a differential input device.

(a) Tie the input HI and LO together.

(b) Apply a 5v, 60 Hz, ADC signal between the tied-together HI, LO and ground.

(c) Observe the output at the test point marked OUTPUT and adjust the RTOCM potentiometer for a minimum output.

(d) When a Common Mode RTO adjustment potentimeter appears on a Buffer Amplifier and the buffer is used as a single-ended input device, the CM RTO potentiometer is to be set to the center of its span.

ZERO (Refer to Figure 90021)

Short E1 (input HI) to ground. Monitor the output at the test point between the RTO CM and GAIN potentiometers with a DVM and adjust the ZERO potentiometer for a 0.000 output.

GAIN (Refer to Figure 90021)

The gain of the Buffer Amplifier in the GM ADC will depend upon the customer's input full scale and output code requirements.

Regardless of the buffer input characteristics, the GM ADC operates on a 20 volt signal swing (+10 to -10 volts). Therefore, the gain of the buffer is adjusted to compensate for the input full scale requirements.

Also due to special requirement of the customer or the A/D System, the buffer may be non-inverting or inverting. The methods for calibration of the gain will vary depending on these amplifying characteristics of the buffer.

(a) Non-Inverting: A gain of 1 buffer with a non-inverting output is calibrated by looking at the input and output differentially on an oscilloscope. Adjust the GAIN potentiometer until there is minimum difference between the input and output of the buffer.

NOTE 1. When the non-inverting buffer gain is other than a gain of 1, it will be necessary to use a divider on the input as in Figure 90022.

The input divider is selected to give an input to the buffer that will produce a full scale output. Measure the input against the output differentially on an oscilloscope and adjust the GAIN potentiometer for a null on the scope.

(b) Inverting: A gain of 1 buffer with an inverting output is calibrated by connecting the input and output per Figure 90023.

R1 and R2 are of equal value. Observe the output at test points P-P

and adjust the gain for a minimum difference as indicated by the oscilloscope.

NOTE 2. When the inverting buffer gain is other than 1, it will be necessary to raise or lower the values of either R1 or R2 to compensate for the gain.

(c) Inverting or Non-Inverting (Alternate Method): Introduce into the input of the buffer a value which will give a 10 volt output. This value is determined by the gain buffer which in turn is determined by the Full Scale of the ADC.

EXAMPLE: If the full scale of the ADC is 5 volts, the gain of the buffer will be two (2) to allow the ADC to operate at a 10 volt level. Adjust the GAIN potentiometer to bring the output of the buffer +/-10 volts.

TOTAL SYSTEMS ADJUSTMENTS

With the assumption that the ADC has been calibrated separately per the procedure in Section 6, it will still be necessary to check calibratiom of the combination ADC-Buffer, ADC-Buffer-Mux, or ADC-S&H-MUX Assembly.

(a) Set or verify that the front panel zero potentiometer is in approximately the center of its mechanical span.

(b) Apply a zero input to the buffer through the rear connector. If a mutliplexer is included, select a single channel. If the multiplexer has an amplifier (Model GMD) in its circuitry, it will have to be calibrated separately before marking these system adjustments. Adjust the buffer zero potentiometer to produce a zero output in the digital output of the ADC System.

(c) Using a near full scale input, adjust the GAIN potentiometer of the buffer to produce an equivalent digital output.

NOTE: The above statements are intended to be touch-up adjustments for the system and are only valid if the ADC has been previously calibrated as an individual part.

0MSH SAMPLE-AND-HOLD AMPLIFIER (Optional) (Figure 90024)

PRELIMINARY

The calibration of the Sample-and-Hold Amplifier should be done after calibration of the Analog-to-Digital Converter. This allows the ADC in the system to be used as a measuring instrument. With reference to the inputs to the Sample-and-Hold, these inputs may be at the rear connector of the unit. However, if the Sample-and-Hold is between the multiplexer and the ADC, it will be necessary to select a multiplexer channel and use that channel for the input. Connect to the multiplexer channel either at the rear connector or remove the channel circuit board and introduce the signal at the common multiplexer output buss.

COMMON MODE

The Common Mode adjustment is necessary for all differential input Sample-and-Hold Amplifiers. Sample-and-Hold Amplifiers with single-ended inputs do not require a Common Mode adjustment. All that is necessary is that the Common Mode Potentiometer (RTCOM) be placed in the center of its span.

(a) Tie the input HI and LO together.

(b) Apply a 5 vac 60 Hz sine wave between the combined HI-LO and ground.

(c) Operate the system so that the unit is in sample or cycling between Sample-and-Hold.

(d) Observe the output at the test point labeled "SH".

(e) Adjust the RTCOM potentiometer for a minimum output.

JUMP ADJUSTMENT (Figures 90025, 90026)

(a) Verify that the ADC timing is correct and the ADC is running at or near the maximum rate.

(b) Adjust the input to 0 volts.

(c) View the output on the test point "SH" with an oscilloscope, and adjust the JUMP potentiometer until both the Sample-and-Hold levels are settled to the same value as pictured in Figure 90026.

NOTE: The above is done best with a sensitive oscilloscope preamp like the 1A5 or the scope input may be placed with the first A Board at the test point marked A2.

PRELIMINARY ZERO AND GAIN SETTINGS

(a) Zero: Set the front panel zero potentiometer to the center of its span. Short the HI and LO together. Using an oscilloscope adjust the zero potentiometer for a zero output at the "SH" test point on the

circuit card. This measurement should be made during the Hold period.

(b) Gain: Introduce a plus full scale signal (the amplifier may have gain) into the amplifier. Observe the test point "SH" with a DVM and adjust for a 10 volt output.

FINAL JUMP SETTINGS

Repeat JUMP ADJUSTMENT (a), (b) and (c).

FINAL ZERO AND GAIN SETTINGS

Repeat PRELIMINARY ZERO AND GAIN SETTINGS (a) and (b).

FINAL CALIBRATION

After the preliminary calibration has been completed, the major transition bit widths, linearity and overall accuracy still must be verified.

DIGITAL OUTPUT CODE OF ADC

The output codes in this final check assume a Two's Complement output code. If the ADC is true bi-polar, it can easily and temporarily be converted to Two's Complement by removing the bottom cover and making the following changes:

(a) Locate the wire that runs from the second "A" board MSB pin 33 to ground. Remove the end of the wire in pin 33 and connect it to the first "A" board (pin 32).

(b) Connect a jumper from the first "A" board pin 35 to the second "A" board pin 36.

After completion of these final calibrations, the wires may be returned to their correct locations.

A One's Complement output code may be checked with this same procedure as if it were a Two's Complement. After making the required adjustments, the width of the combined + and - zero's are adjusted to be two bits wide. No actual internal logic exists to remove the extra

zero code (- 11 111 111 111 111) for non-existent "minus zero" characteristic of the Two's Complement code. All examples shown are for a 4 bit and sign resolution. The same adjustments apply to lesser resolutions (down to 10 bits).

INITIAL SET-UP (Figures 90027, 90028)

(a) With the rear panel power switch in the OFF postion, make all the necessary input and output connections. This includes control lines for the multiplexer (if present), AC power, analog inputs and external clock signal. If the multiplexer inputs are present, connect them in groups per Figure 90027 or 90028.

NOTE: The analog inputs must never be left open.

External control lines unless otherwise specified are standard TTL levels. Pulse widths are 100 nanoseconds minimum. Unused digital input control lines (reset, etc.) must be tied to digital ground.

(b) Connect a voltage calibrator or a variable DC source with DVM to the analog input(s) and adjust the output of the calibrator for zero volts.

(c) Place the power switch (rear panel) to the ON position and allow an one-half hour warm-up.

(d) Adjust an external clock pulse generator to the maximum conversion rate of the ADC or system.

(e) Using an oscilloscope, recheck the timing pulses for the correct settings (see Section 12 for the Test Report).

(f) Check the plus and minus 10 volt reference supply.

(g) Set the multiplexer channel to "0" if applicable.

(h) Verify that the front-panel indicators are operating by varying the analog input.

(i) Place the calibration covers (see the note on covers in the Introduction of Section 6) on the ADC and allow the airflow to stabilize for 5 minutes minimum.

These covers are especially made at our plant and have slots machined in them to permit access to the adjustment potentiometers. If one of these covers is used, one must still cover all of the remaining slots that are not being utilized for adjustments. If no special cover is available, adjustment may be made by removing the cover only for the adjustment. When this method is used, time should be permitted for the airflow to normalize after the cover has been replaced.

SIXTEEN (16) POINT LINEARITY

The method used to determine corrections required is to plot a 16 point linearity curve and compare it with the theoretical curve. Points plotted are at 1/4 scale increments from minus full scale to plus full scale. Actual transitions are plotted on both sides of major bits and near full scale. These points provide a picture of which adjustments are required for final calibration. This proves to be especially true when the actual bit is missing due to misadjustment.

Known D.C. voltages are applied to produce codes listed in Table 90050. All codes that are 1/8 scale increments are not normally plotted unless a problem condition is present. Only the +/- 7/8 scale transition points are plotted to verify that transition width. This also allows a better drift setting of the 4th A board zero at temperature. The specific points on Table 90050 were selected to provide an easily recognized binary pattern.

Voltages required to produce these patterns are recorded and compared to the theoretical values. The algebraic differences, in millivolts, are plotted as errors on a vertical axis (See Figure 90029). The horizontal axis show analog inputs from minus to plus full scale.

Points are plotted from minus to plus full scale in sequence per Table 90051. Points on each side of a transition point are plotted as though they occured at the transition point. This means that transitions on both sides of a bit are plotted at the same horizontal coordinates.

Example: -2.5080 & -2.4877 (typical values) are plotted at -2.5V. The important part is to connect points in proper sequence. If the typical readings are the same as the theoretical values, a straight line with 0 errors like Figure 90029(B) would result. With the transitions at zero width, any change due to drift or component aging could result in a reversal or 'flipped' transition. This in turn could result in a missing bit. To avoid this, the transition width is purposely adjusted to a width of approximately .8mv. Figure 90029(A) shows all widths at .8mv.

The transition errors plotted on both sides of any bit must always be in a minus to plus direction. If not a correction must be made. When making corrections always make adjustments to least significant bits first since they affect more significant ones. Example: If 1st, 2nd and 3rd 'A' board adjustments are required, the 3rd 'A' should be adjusted first, then the 2nd, then the 1st. It is normally a good practice to plot a curve after each adjustment to be sure only the intended changes were made and no others.

In Figure 90029(A) all errors are .4mv in the correct directions.

Slopes of the segments should all be similar. If the slopes are not similar, certain adjustments may be made to correct the slopes (see K2 and K1 adjustment curves).

Observe symmetry of adjustments in curves in Figures 90031 through 90042.

The four important items displayed on these curves are:

1. Transition widths = W
2. Slopes
3. Zero Offsets
4. Gain Errors (Slope of entire curve)

For this reason, no attempt is made to correct these curves to the ideal theoretical curve (Figure 90029(B). The curve instead, is corrected to one similar to Figure 90029(A), the Ideal Practical Curve. Real curves do not usually look as perfectly symmetrical as the Figure in Figure 90029(A), however, all points must be within the overall accuracy of the ADC under test.

Figures 90031 to 90043 B & C show the affect of adjustments on the first three most significant bit boards on the overall curve.

NOTE: The 4th 'A' board affects the 1/8 scale increments in a similar manner. The theoretical values are included in the computer printed work sheet (Figure 90030).

In Table 90050 the codes always display the same pattern for the last 5 bits.

BIT 16 ON
BIT 8 OFF
BIT 4 OFF/ON
BIT 2 ON/OFF
BIT 1 ON/OFF

The mark (____*) on the last 3 bits indicates a binary 3 4 change. At this point the code is alternating from 3 to 4 or 100 to 011.

Running at normal speed the change can be observed by an equal brilliance of the last 3 indicators. As the input is changed by a small amount the 3 or 4 code will come on. It must not be confused with the binary 7 where all three indicators are solid 'ON'. If the exact center is desired, a DC voltmeter may be connected across the '4 bit' to digital ground. Adjust input so that the 4 bit is on solid. Note voltage. When the meter indicates 1/2 the noted voltage, a 50% duty cycle will be present. This means the 4 is on 1/2 the time which in turn means the 2 & 1 are ON the other 1/2. This procedure is usually only required where noise makes it difficult to determine the transition point.

ADJUSTMENTS TO CURVES

Adjusting the Z1 and the Z2 potentiometers will remove any transition errors present (see Figure 90018). These corrections should be made to approach the Ideal Practical Curve in Figure 90029(A).

The actual curve, although not as perfectly shaped as the Ideal Curve, must be within the tolerance of the ADC. If the ADC is to be temperature cycled, retain this curve after it is corrected and mark it 25 C.

Errors at the transition points should always go from minus to positive

as input goes from negative to positive: Example points [2] & [3] (Figure 90029A). The error at point [3] must be more poitive than the error at point [2]. If not, corrections are made as required.

Transition width adjustments affect more significant bit transitions. Therefore an adjustment to the 3rd A Board zero will require readjustment of the 1st and 2nd A board zeroes. Z1 and Z2 adjustments do not affect the slope but slope adjustments do affect slope and zeroes of more significant boards.

After making a change, it is best to re-plot the curve to be sure the desired affect was obtained.

THIRD 'A' BOARD ADJUSTMENTS

The Z1 pot on the 3rd 'A' board will move the sections from [1] to [2], [7] to [8], [9] to [10], and [15] to [16] as shown in Figure 90031.

Moving the Section [1] to [2] will affect the other sections in a like manner. Thus, if the transition width 'W' for the third board was to be widened by 1 mV, a 1 mV change with the Z1 would be required. This adjustment must be made from the proper side, i.e. the code at pt [2], [7], [10] or [15].

The Z2 is used to widen Sections [3] to [4], [5] to [6], [11] to [12], and [13] to [14]. These voltage inputs must correspond to the pt [3], [6], [11], or [14]. The amount of change made will be the amount that

the transition width is widened or narrowed, reference Figure 90031.

NOTE: In Figure 90031 and 90032 that changing W at -3/4 scale (-7.5V) causes an equal change at +/- 2.5V (1/4 scale) and +7.5V (+3/4 scale) points. It also affects zero transition widths.

(b) Z1:

The Z1 adjustment is only used where positive voltage is at the input of the third A board. It is used at the +/- 1/4 & 3/4 scale points but may only be adjusted one side of the transition. At 3/4 scale points [2] or [15] must be used. At 1/4 scale points, [7] or [10] must be used. If the -7.5080 transition is changed to -7.5085 or .5mV more negative then the -7.4877 transition is unaffected and the transition width W increases from -.8 to -1/3 mV error. Example: Figure 90032. If the -7.5080 transition is changed to -7.5072 the width W becomes '0' as in Figure 90032.

(c) K1:

The K1 adjustment changes slopes per Figure 90033B or 90033C. The adjustment is made from the end points: [1] or [16] or center points [8] or [9].

Example Figure 90033B:

At [1] -9.9877 is increased to -9.9867 or 1 mV more positive with K1

pot.

NOTE: The 3rd A K1 pot affects the zero transition width. In Figure 90033B it increases the transition width. The same change would result from adjusting points [8] or [16] 1 mV negative or point [9] 1 mV more positive.

Figure 90033B shows the opposite direction change.

NOTE: K2 shows a gain slope change where Z2 and Z1 adjustments show an offset change.

(d) K2:

The K2 adjustment changes slopes per Figures 90034B and 90034C. Adjustments are made from 1/2 scale transition.

EXAMPLE: Figure 90034B is obtained from 90034A by going to point [4] or [12] and adjusting K2 for about -.6mV more error, or going to point [5] or [13] and adjusting for a positive .6mV error increase. This adjustment changes the width of the +/- 1/2 scale transitions.

SECOND 'A' BOARD ADJUSTMENTS

Adjustments are similar to the 3rd 'A' board but are made at different points.

The Z1 and Z2 potentiometers are used to correct +/- 1/2 scale transitions. The affects are shown on Figure 90035B and 90035C.

If the -5.0080 transition is changed with the Z1 pot to -5.0084 (-.4mV) the -4.9877 transition does not change. This widens the transition by the amount of change made.

The Z1 adjustment, like the 3rd board, must be made at the side of the transition with a positive voltage into the board. In this case point [4] transition or the point [13] transition. The K2 adjustments are made at points [5] and [12]. The K1 adjustments are made at the +/- f/s transitions (90037 B,C). The K2 adjustments are made at the +/- zero transitions (90038 B,C).

FIRST 'A' BOARD ADJUSTMENTS

Z2 pot offsets the half of curve with the negative voltage input per Figure 90039B. The Z1 adjustment offsets the half of the curve with positive voltage into the board (90040 B,C).

This means with an inverting buffer between the input and the first 'A' board that the negative transition (normally zero -.0080 for example) is used.

The K1 potentiometer pivots the half of the curve with a positive input to the 1st 'A' board about zero. The corresponding full scale transition is used for adjustment. Reference Figures 90041B and C.

The K2 potentiometer pivots the half of the curve with a NEGATIVE input to the 1st 'A' board. The corresponding full scale transition is used for adjustment. Reference Figures 90042B and C.

For future temperature checks run a 16 point linearity and mark it 25 C.

HIGH TEMPERATURE

(a) Raise the ambient temperature of the system to 50 C or 55 C as required. Allow the unit to soak at this temperature for a minimum of 1/2 hour.

(b) Run a 16 point linearity curve plus the transition points around +/- 7/8th scale. (Refer to 16 point linearity).

(c) Compare these results with the room temperature curve. Using the available drift potentiometers, Z1 and Z2, make adjustments to return the high temperature results to the results obtained in the 25 C run.

At high temperature the DRIFT potentiometers on the 'A' boards allow corrections to be made corresponding to room temperature Z1 and Z2. Adjustments are made starting with least significant bit (usually the A4 board at a 1/8 scale transition) towards the msb (A1). The curve is adjusted to be as close as possible to the one at room temperature.

In addition to the 'A' boards, the buffer/or sample-and-hold have zero

Suppose with the buffer drift set to Zero, the curve is approximately as shown (Figure 90044B). Zero transition points [8], [9] would be approximately

(8) -.0066 or +1mV error

(9) +.0137 or +1.4mV error

The 1st 'A' board Z1 and Z2 drift potentiometers can be used to offset the curve back around zero as follows:

First determine whether the buffer or S/H is inverting. The Z1 drift adjustment is only made with positive voltage into the 1st 'A' board and only affects the corresponding half of the curve. The Z2 drift adjustment affects the half of the curve with the negative polarity input. Reference Figures 90039B, 90040B and C.

If the buffer is inverting, adjust analog input for +0.123 volts which is the room temperature value (Figure 90044A). Adjust 1st 'A' TC2 potentiometer for ___*. This will bring the right half of the curve down 1.4mV to its proper position. Now adjust analog input for -.0080V. Use the 1st 'A' TC1 potentiometer and adjust for the proper code for the [8] transition -11111111110___*. The curve should as shown in Figure 90044A.

NOTE: With a non-inverting buffer the [8] transition would be corrected first. This would result in a curve like Figure 90044D. Using TC2 adjust point [8] is moved from -.0066 (+1mV error) to -00.80 (-.4mV error). The TC1 potentiometer can now be used to bring point

[9] back to its room temperature value.

Figures are normally plotted with errors at 1mV/div. Reading errors and input errors define 1mV/div as a good practical limit.

Figure 90045 shows a typical curve with +/- 7/8 full scale points plotted to check transition width set by 4th 'A' board.

The only adjustments that cannot be made at high temperature are the slope changes on the 'A' boards. Since slope changes do affect transition widths, 'over-corrections' with the Z1 or Z2 drift potentiometers must be employed. If these do not provide enough adjustment to bring the curve within tolerance, the unit should be returned to room temperature and the board(s) with problems should be repaired.

(d) Allow the unit to remain at this high temperature for at least 1/2 hour and repeat the curve to verify the stability.

ROOM TEMPERATURE CHECK

(a) Allow the unit to settle at room temperature for at least one hour.

(b) Repeat the 16 point curve and mark this 25 C #2.

(c) The results should be nearly the same as the one marked 25 C.

(d) If the room temperature curves are nearly the same as the high temperature curves, the temperature compensation is correct.

(e) If the curves are not the same, touch up the curves at room temperature and repeat the high temperature drift run.

LOW TEMPERATURE

(a) Record the curve for the room temperature.

(b) Lower the temperature to O C and allow at least 1/2 hour to settle.

(c) Plot the 16 point curve and verify that all points are within over-all tolerances.

(d) If an incorrect transition is obtained, but only a small amount, a determination of whether a drift adjustment should be made or the ADC should be returned to room temperature where the bit may be corrected by the regular zero potentiometer must be made. In either case, a rerun on high temperature must be made.

(e) Return ADC to hi temperature to dry out if moisture was present. Allow 1/2 hour minimum time to settle.

(f) Return ADC to room temperature and allow a 1 hour minimum time to settle. Repeat 16 point curve. If specific bit is to be widened, make required adjustments to do this and others as required to correct

curve.

SECTION 7

TROUBLE SHOOTING PROCEDURES

SYSTEM TROUBLE SHOOTING

This section describes the recommended procedures for trouble shooting the GM Series Multiplexing Analog-to-Digital Conversion System. The procedures have been separated into three major building blocks of the system i.e. (1) the power supply, (2) the multiplexer, (3) the analog-to-digital converter.

Prior to beginning the trouble shooting, make certain that all instrumentation associated with the system is checked to determine that the apparent problem is within the GM System. Check that all external addressing is correct and that the input/output, analog and digital lines are properly terminated.

Calibration adjustment potentiometers and capacitors are preset at the factory. No adjustment of these controls should be attempted until a check of the system has been made.

To prevent damage to the semiconductors the main power should be turned off before plugging or unplugging any circuit card.

In some cases, concerning the Sample-and-Hold Buffer Amplifier, timing board, or high resolution bit boards placing the board on an extender card will effect the normal operation of that board. All boards should be in their slots when any critical parameters are measured such as system timing, sample-and-hold adjustments and final calibration.

This system has a temperature sensitive switch mounted internally at the rear of the chassis. This switch is designed to interrupt the main power should the internal temperature of the system rise to 70 C. This temperature switch is self-resetting and will restore the power when the temperature is again lowered to 55 C.

GENERAL TROUBLE SHOOTING EQUIPMENT

Equipment recommended for trouble shooting consists of the following:

(a) A stable DC analog voltage source, variable over the range of +/- full scale input voltage or +/- 10 volts whichever is greater. The voltage resolution should be at least 25% of the least significant bit. The source impedance should be less than 1000 ohms.

(b) Oscilloscope, Tektronix 545A, with 1A5 and CA Preamplifiers, or equivalent.

(c) Five-digit digital voltmeter, differential voltmeter, or equivalent. The accuracy should be at least twice that of the system being tested.

(d) Triangle wave generator with a capability of 20 volts peak-to-peak into a 470 ohms load at 1 kHz.

(e) VOM such as Simpson 260.

(f) Pulse generator to provide clock pulses of an equivalent in amplitude width and frequency to the normal system operating pulses.

(g) Printed circuit card extender, bit board extender (Part No. 52315) and Sample-and-Hold Buffer extender (Part No. 52318). All three are supplied with the unit. (Part No. 52315 and 52318 may be replaced by a single extender Part No. 52330.)

FAULT INDICATION	POWER SUPPLY CHECK
Loss of Power	Line fuse, power, ON-OFF Switch, High temperature which may have caused temperature sensor to remove power.
Loss of Display	Assuming that the ADC is operating correctly, and the failure is other than an individual LED, the lamps are connected through resistors to the common 5 volt supply. Check the 5 volt supply. The display is accomplished by using an LED device, they are driven by the output data through inverters mounted on the lamp display board. To turn the lamp on the inverter output must go false. Check both input drive to the inverter and the output of the inverter. If the above checks prove "OK" then the lamp is at fault.

Non-Operating System

First check to see that all plug-in boards are seated properly. If the above check has been made and the problem still exists make a check of the plus and minus 10 volts and the plus and minus 33 volts. Refer to Figure 90049 for these test point locations.

ADC PROBLEMS AND POSSIBLE SOLUTIONS

Refer to the Block Diagram, Figure 90047 for a flow-chart relating to ADC problems and their solutions, by category.

Faulty Positive Reference Power Supply

The reference power supply provides a precisely regulated, highly stabilized reference voltage for use in the ADC bit boards. It consists of two differential amplifiers. Each is an operational amplifier with its own feedback loop. The primary standard reference is a zener diode. The reference control -10v adjusts the output voltage of the minus supply and the +10v control adjusts the output voltage of the plus supply.

A faulty positive reference supply will have the following indications:

(a) An error in the digital information (gain error).

(b) A zero offset which cannot be removed with front panel adjustment.

Check the +10 volt reference supply at the test points on the circuit board. It should be adjustable with the gain potentiometer located on that board and labeled +10v.

Faulty Negative Reference Supply

A faulty negative reference supply will give a Zero error, except that the Gain will not be affected. Make the same checks as above using the negative test point (-10v) and adjustment potentiometer (REF).

Incorrect Calibration of Buffer or Sample-and-Hold Amplifiers

Incorrect data and zero offsets may be due to adjustments in the analog area of the ADC such as the buffer or the Sample-and-Hold Amplifiers.

Check the calibration of the buffer or Sample-and-Hold Amplifiers to see if the problem exists in this area.

Defective Bit Board

An incorrect digital output may be caused by an uncalibrated bit board or by some malfunction of a bit board.

Check the bit board in question by using the calibration procedure described in Section 6 (only that portion describing the method for introducing a signal into the bit board in question on the plain extender, Part No. 48289), so that test points of individual parts on the board may be available.

Introduce a 1000 Hz triangular wave of a peak-to-peak value of 20v (see Figure 90048) into the bit board and view the output of the board at A1

and A2.

Trigger the ADC for a conversion at a rate of 10 kHz. The result is shown for a good board in Figure 90048. Also refer to Figures 90013 and 90014 for clarification.

TROUBLESHOOTING THE MULTIPLEXER CARD

Refer to Section 2 of this manual for the operation of the multiplexer switch and its associated circuitry. Decide whether the problem which exists is isolated to a particular channel or is common to all multiplexer channels.

Each multiplexer card has its own power regulator and is independent of the other multiplexer cards in this respect. If a particular channel is not functioning, or if only one channel is operating correctly, manually select that channel and monitor the multiplexer drive (see Figure 90010), check to see that the proper drive signal appears at this test point.

If a drive signal appears at this point, trace the drive and check to see that the correct drive appears at the gate of the FET. The gate is held at a negative potential when the FET is in the OFF state and when it is turned ON, the FET gate is allowed to slew to the same potential as the input signal of the multiplexer.

If the negative potential that holds the gate in the OFF state is

functioning properly and the gate does not assume the potential in the input signal, the problem is probably associated with the unity gain amplifier (see Figure 90010).

If all of the above items checked are functioning correctly, the problem is probably a defective FET semiconductor.

SPECIFIC MULTIPLEXER PROBLEMS

Below are some problems that may occur. The problem may affect the entire unit and symptoms may appear on all channels, but are caused by a single channel.

Shorted FET Semiconductor Switch

A FET switch that is shorted or fails to turn off completely will provide added analog information to the multiplexer output. If the unit is an ADC/MUX combination, the information out of the ADC will be erroneous and it may appear that the ADC is at fault. When a shorted FET switch is encountered, it may not be immediately apparent. The front panel indication may function correctly and the logic associated with the shorted FET switch may operate correctly, but the analog information on the multiplexer will be incorrect due to the addition of the information of the defective channel.

Open FET Semiconductor Switch

The front panel indication of a selected channel will not always mean that a particular channel is operating properly.

To check the operation of a single channel, move the MODE switch to the SEQUENTIAL TEST MANUAL position. Set the MUX ADDRESS to cover all channels. Bus all inputs to the same known analog input and monitor the multiplexer output. Manually sequence through each channel, noting that the proper analog signal appears on the multiplexer output for each channel selected. When the correct signal fails to appear on the multiplexer output, the defective channel has been located. Make sure that the test for correct drive for that channel has also been made.

SECTION 8

ILLUSTRATIONS

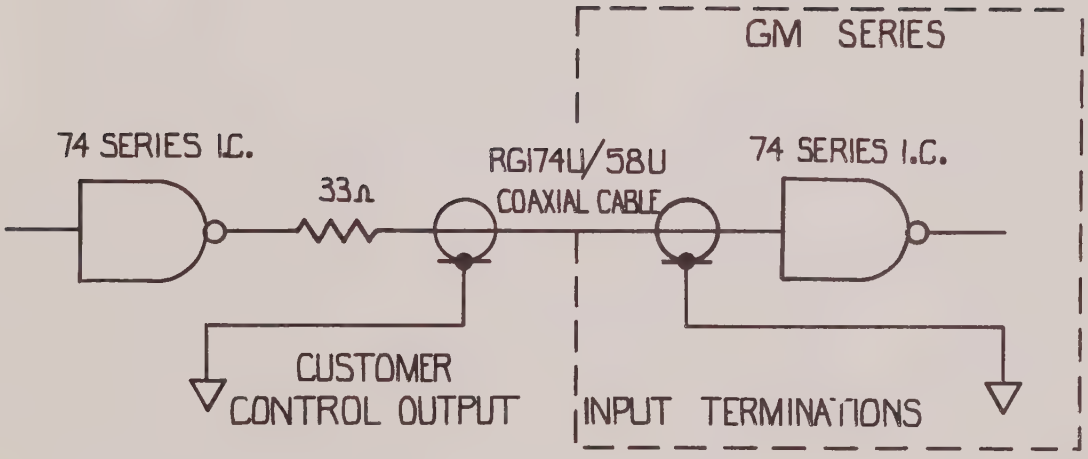


FIGURE 90000

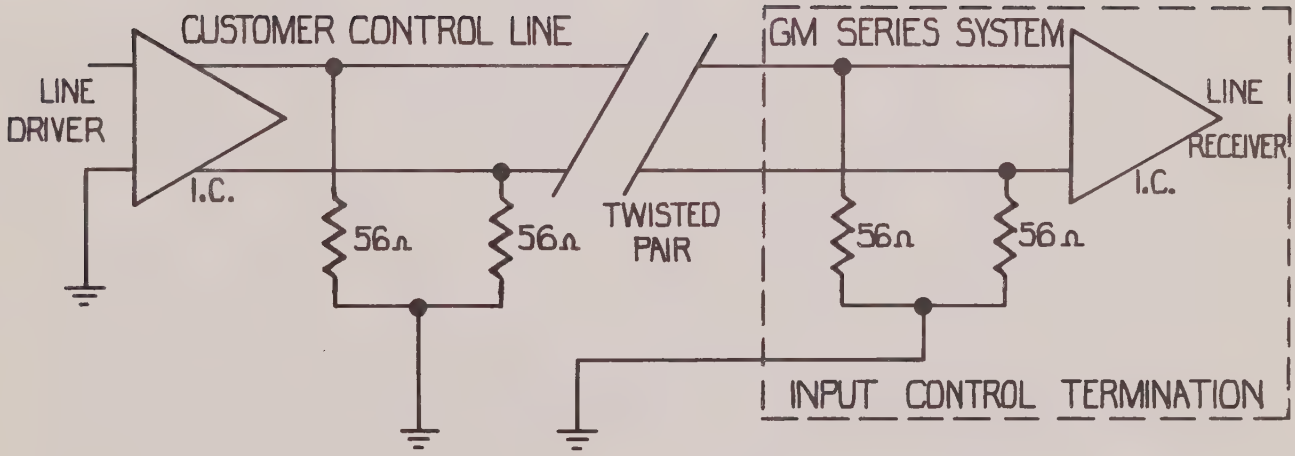


FIGURE 90001

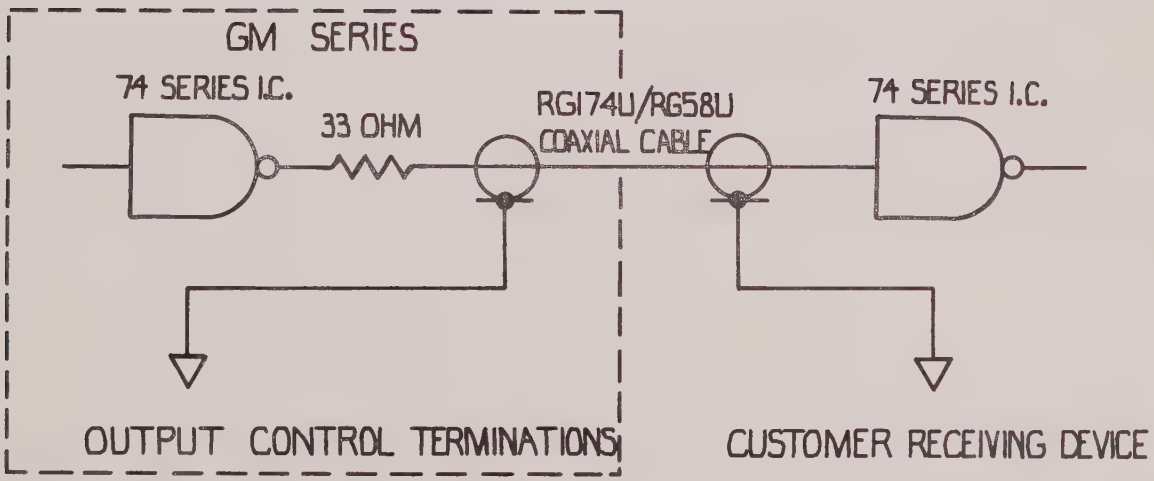


FIGURE 90002

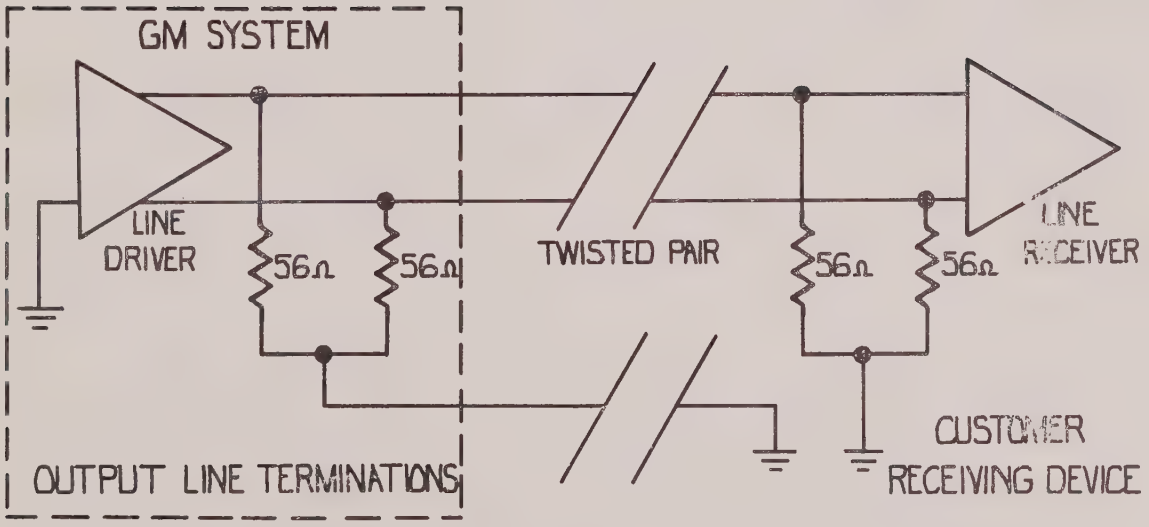


FIGURE 90003

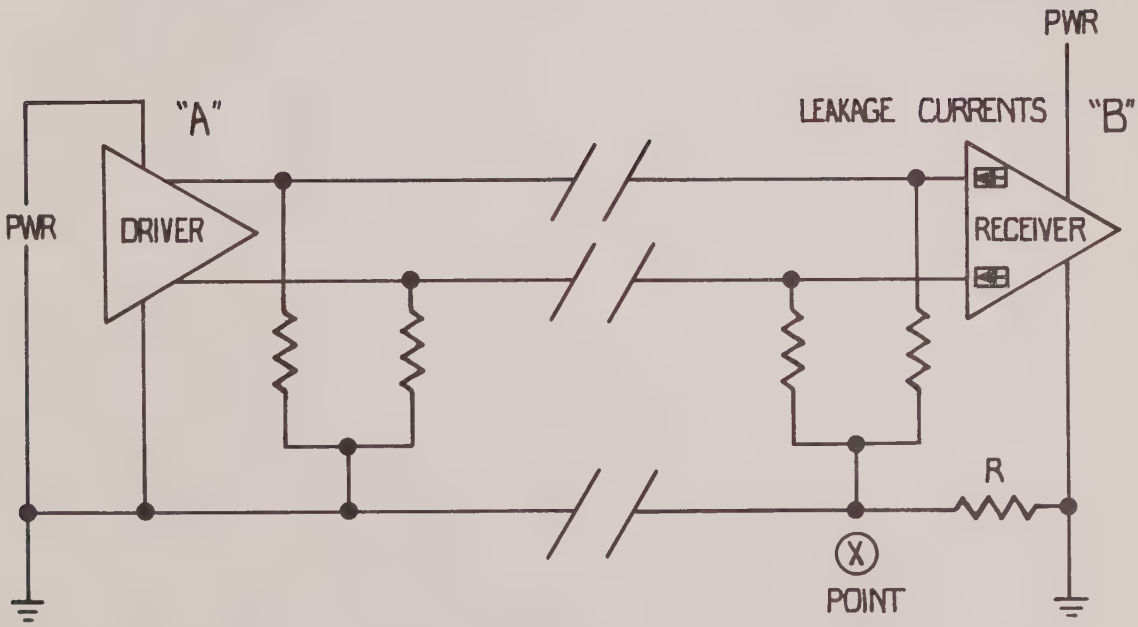


FIGURE 90004 Common Mode Terminations

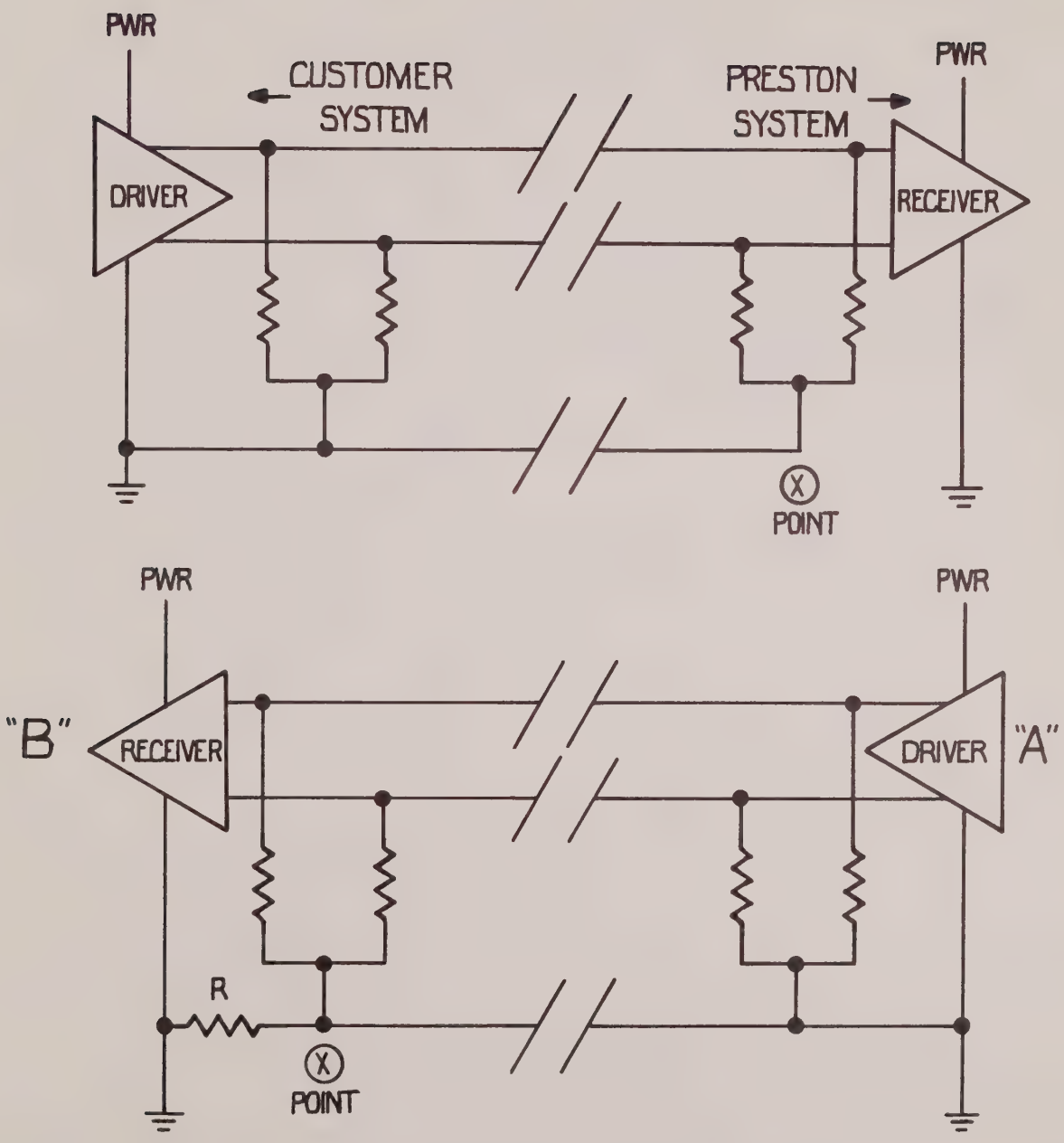


FIGURE 90005 Common Mode Terminations
Two-way Communications

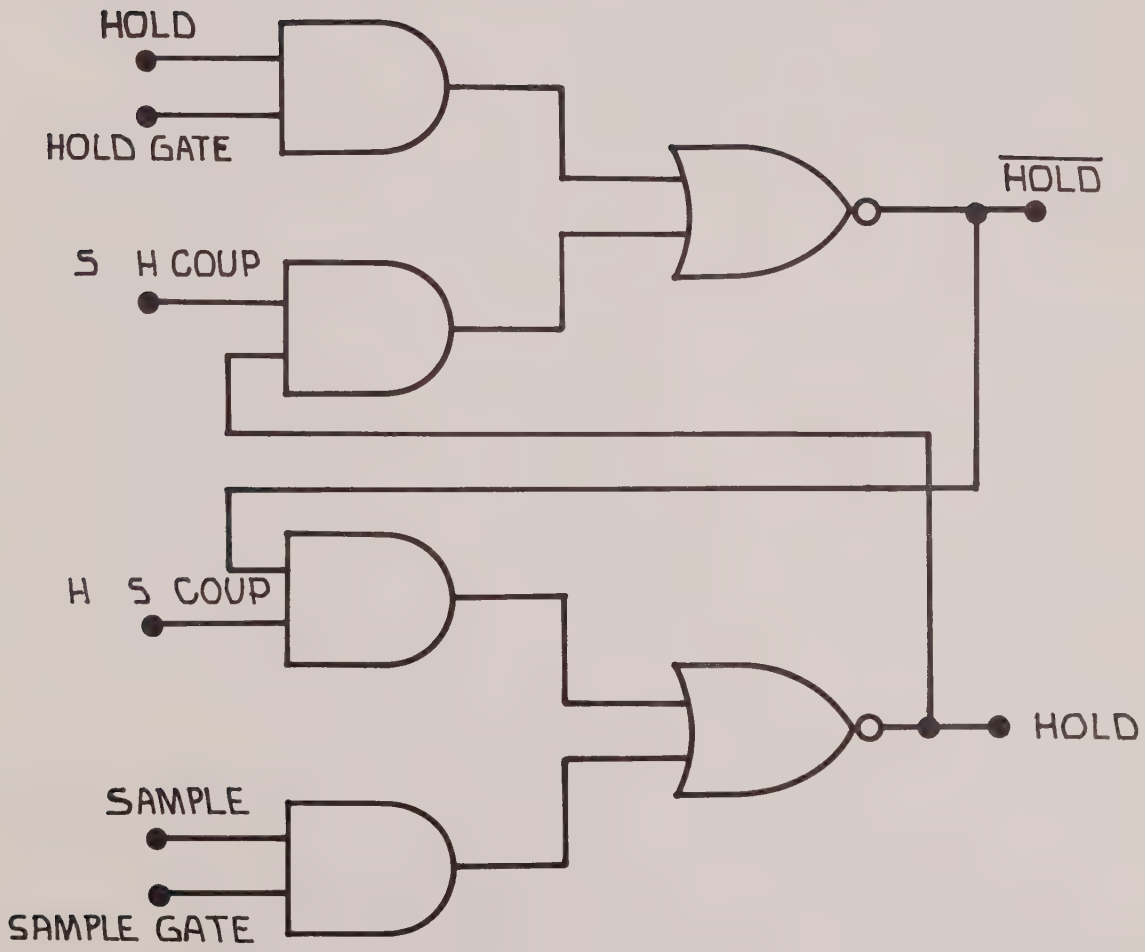


FIGURE 90006

	HOLD	HOLD GATE	SH COUP	SAMPLE	SAMPLE GATE	HS COUP
PULSE TO SAMPLE	D	T	T	D	T	T
PULSE TO HOLD	T	D		T	D	
DRIVE TRUE FOR SAMPLE	X	0	T	D	T	F
	0	X		T	D	
DRIVE TRUE FOR HOLD	D	T	F	X	0	T
	T	D		0	X	

X = UNUSED

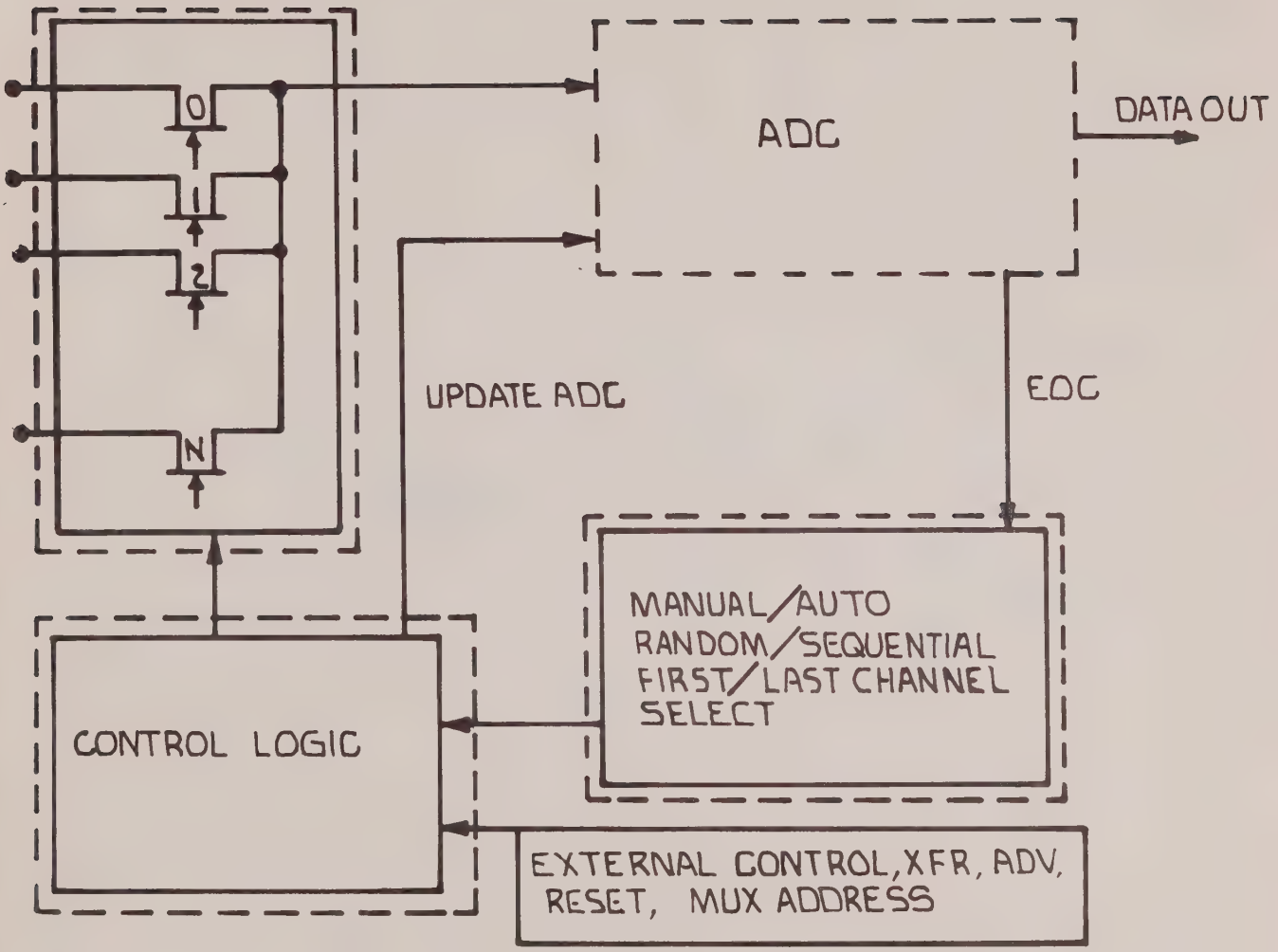
0 = KEPT AT LOW LOGIC LEVEL

T = TRUE

F = FALSE

D = DRIVE

FIGURE 90007



DOTTED LINES INDICATE THE MULTIPLEXER AND ITS CONTROLS MAY BE MOUNTED IN THE SAME MODULE AS THE ADC OR MOUNTED IN A SEPARATE MODULE DEPENDING UPON CUSTOMER REQUIREMENTS

FIGURE 90008
MULTIPLEXER MODULE
BLOCK DIAGRAM

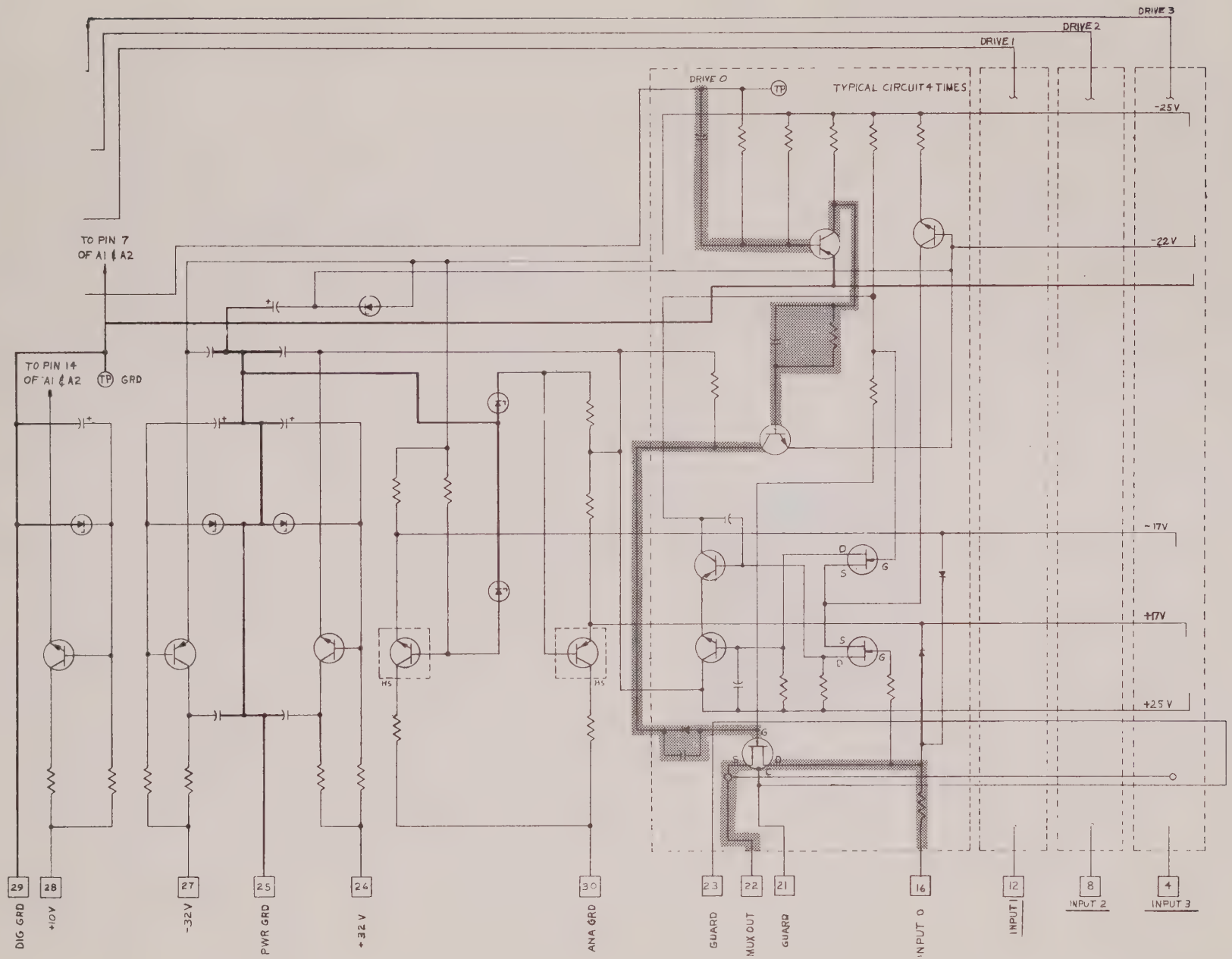


FIGURE 90009

MULTIPLEXER SWITCH

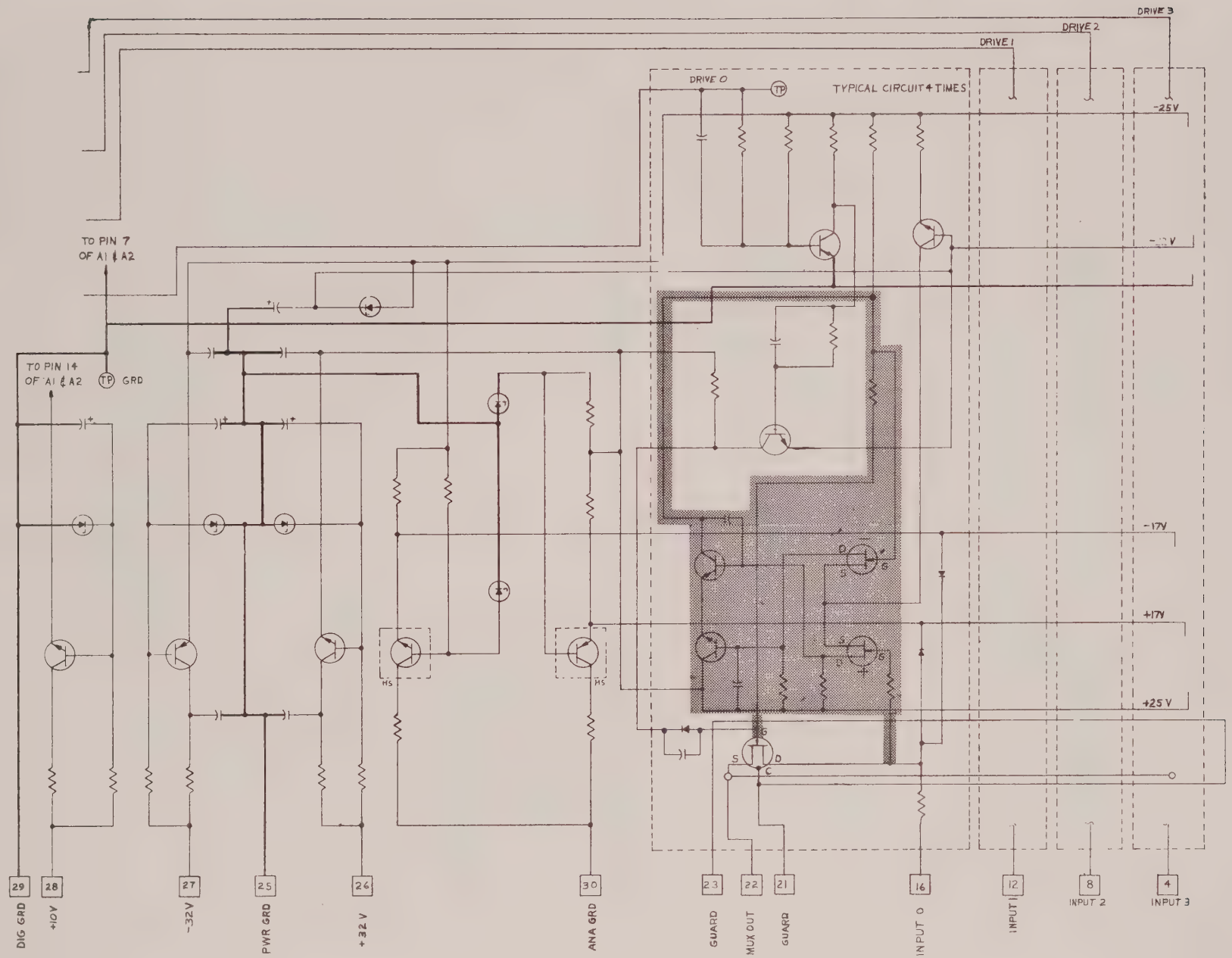


FIGURE 90010

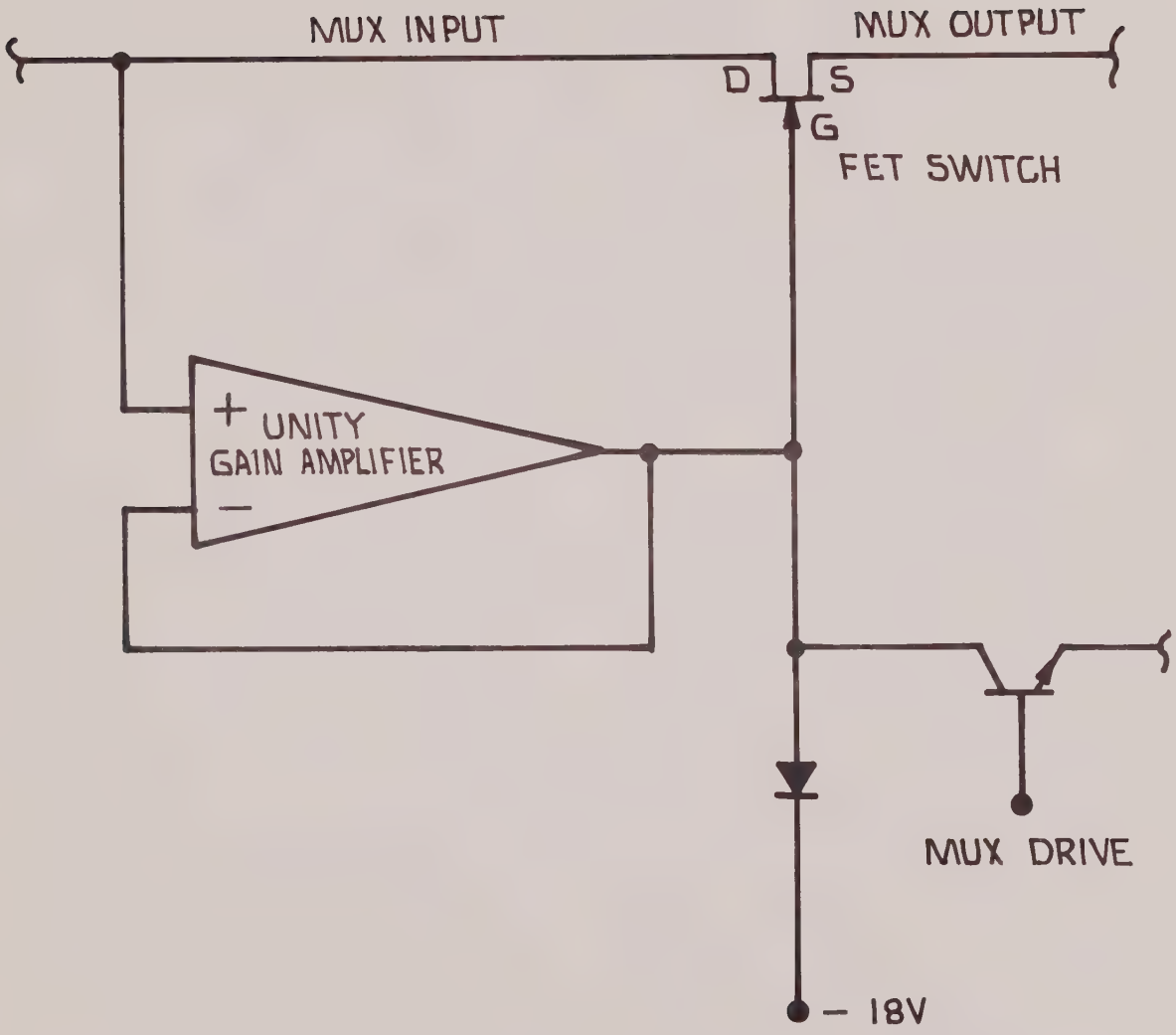


FIGURE 90011
MULTIPLEXER SWITCH
BLOCK DIAGRAM

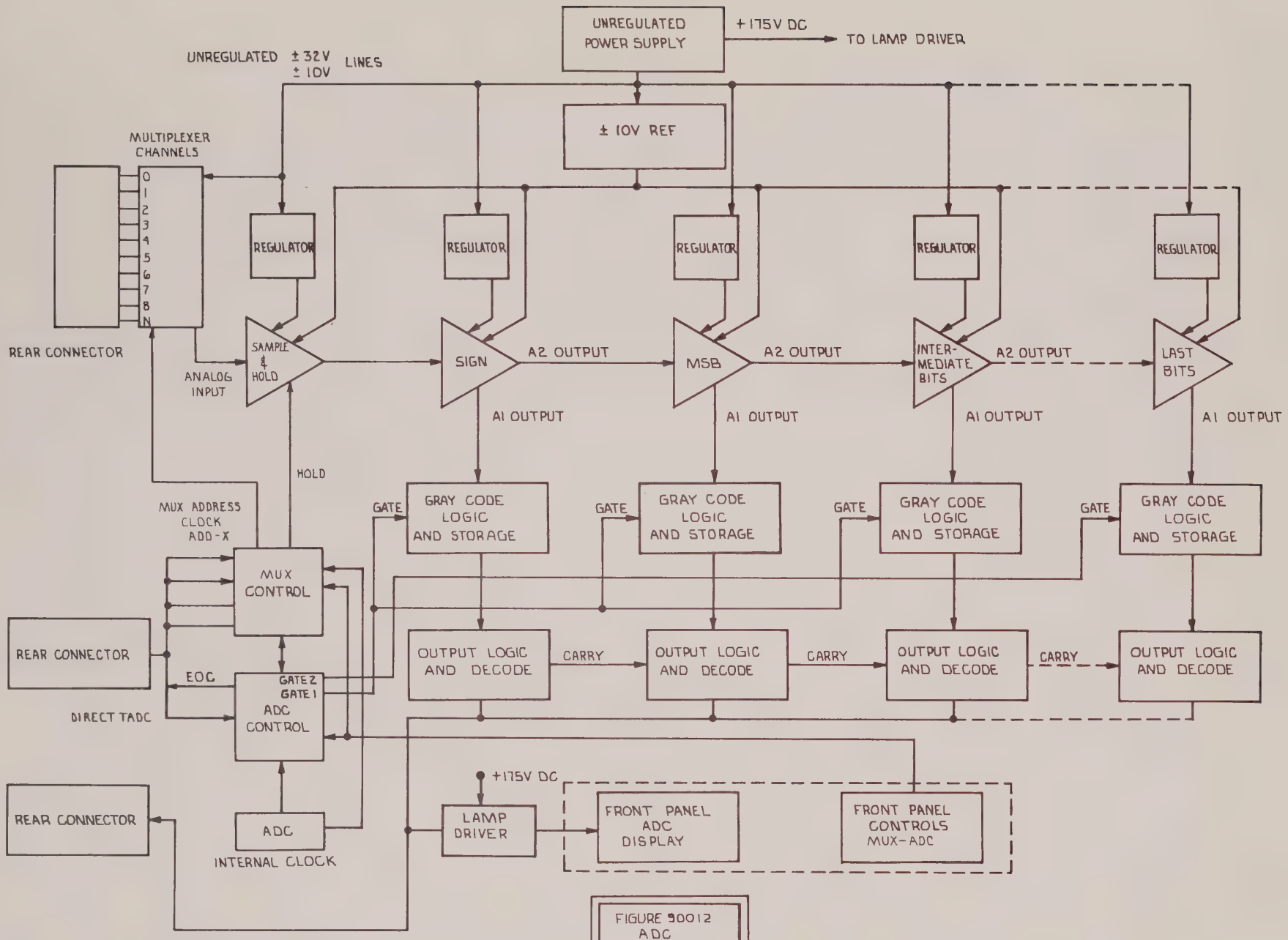


FIGURE 90012
ADC
BLOCK DIAGRAM

GMAD - SAMPLE & HOLD - MULTIPLEXER

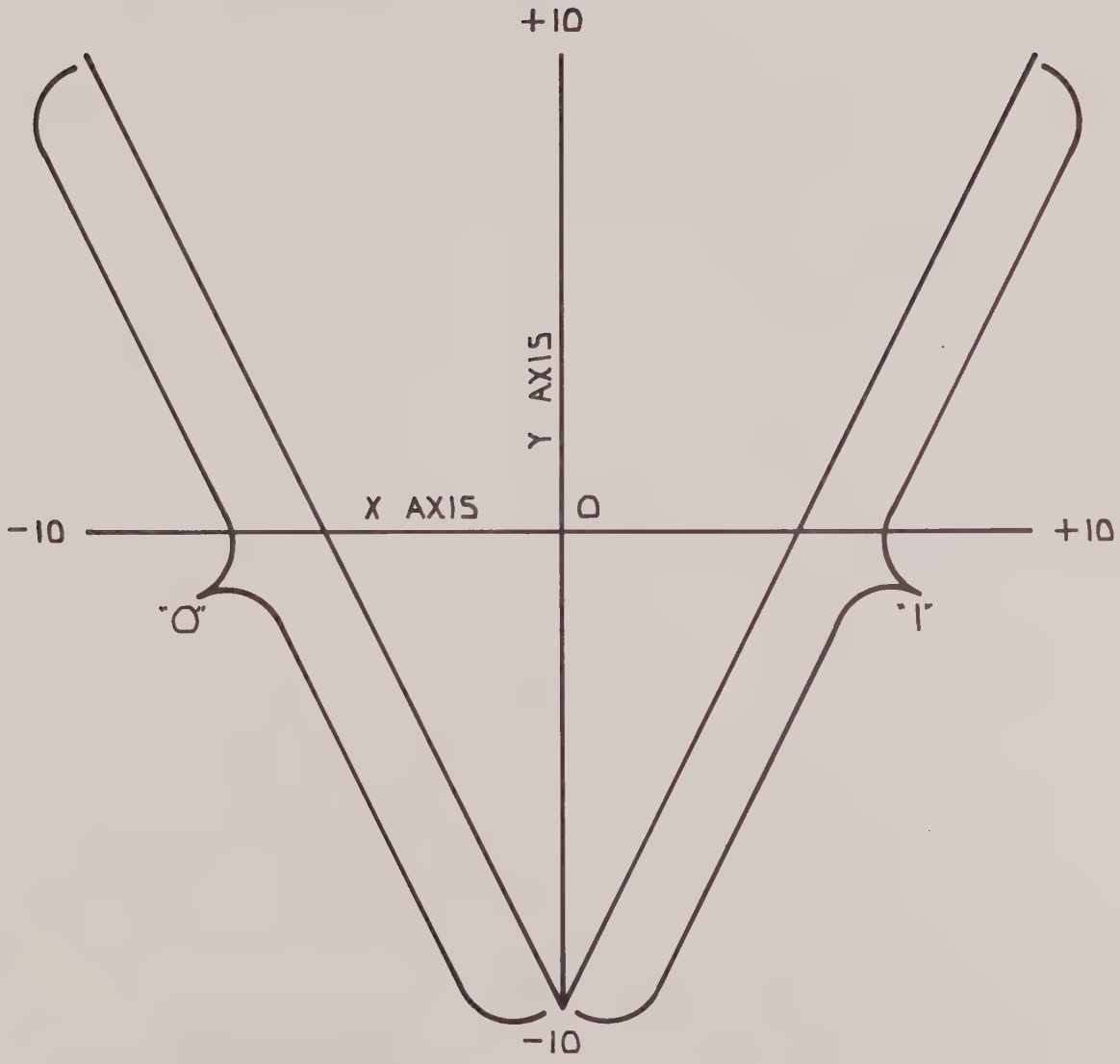


FIGURE 90013

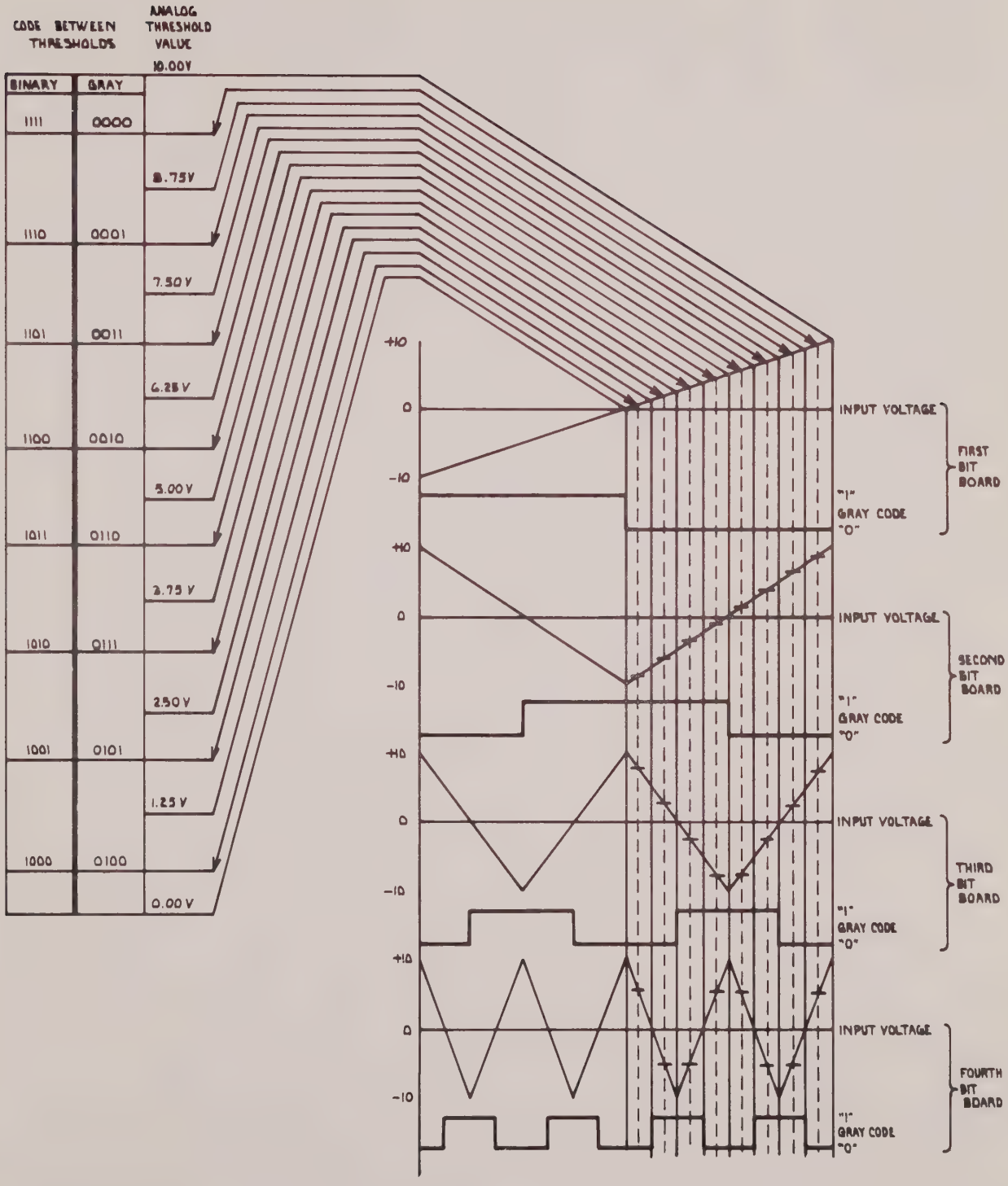


FIGURE 90014

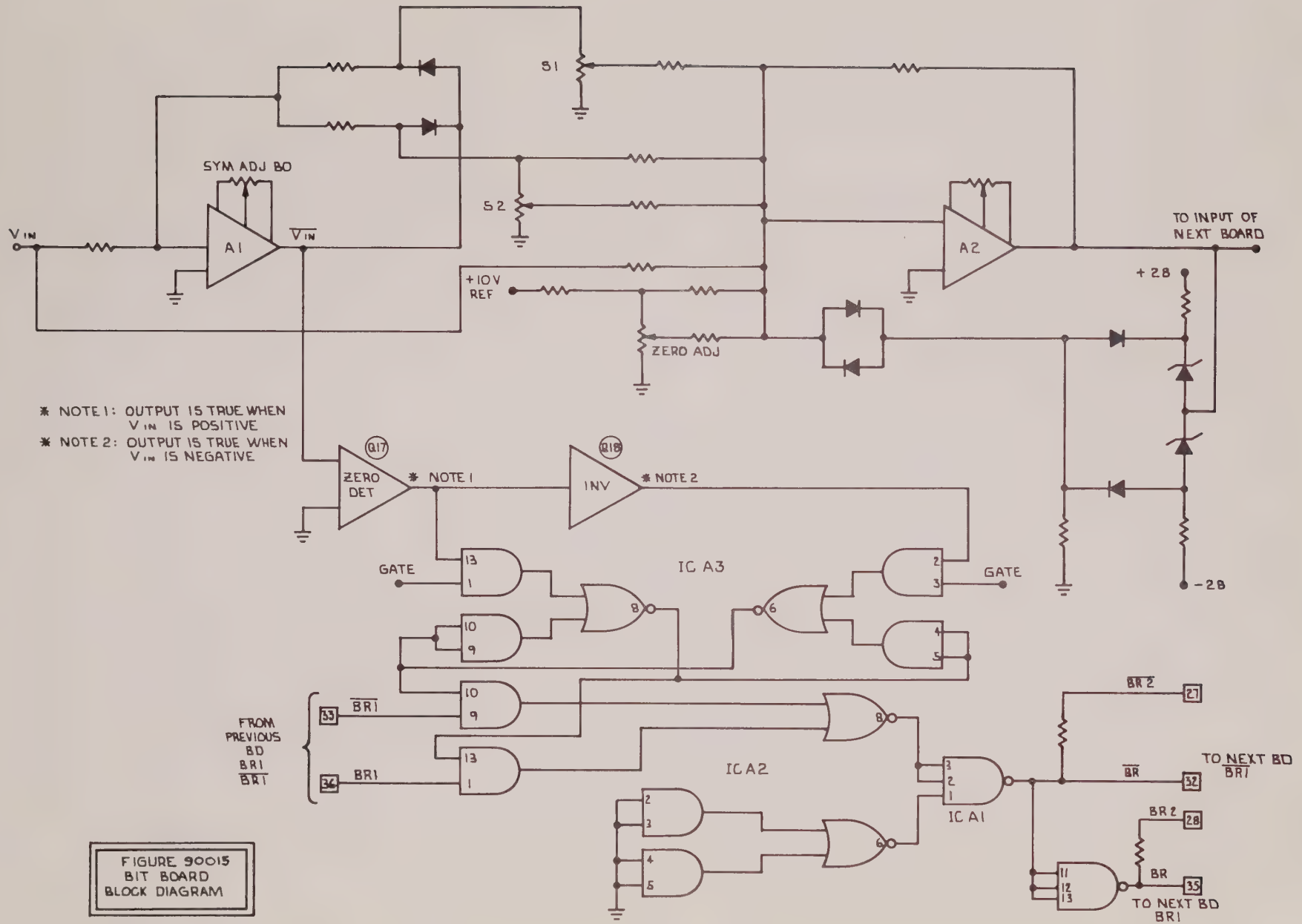


FIGURE 90015
BIT BOARD
BLOCK DIAGRAM

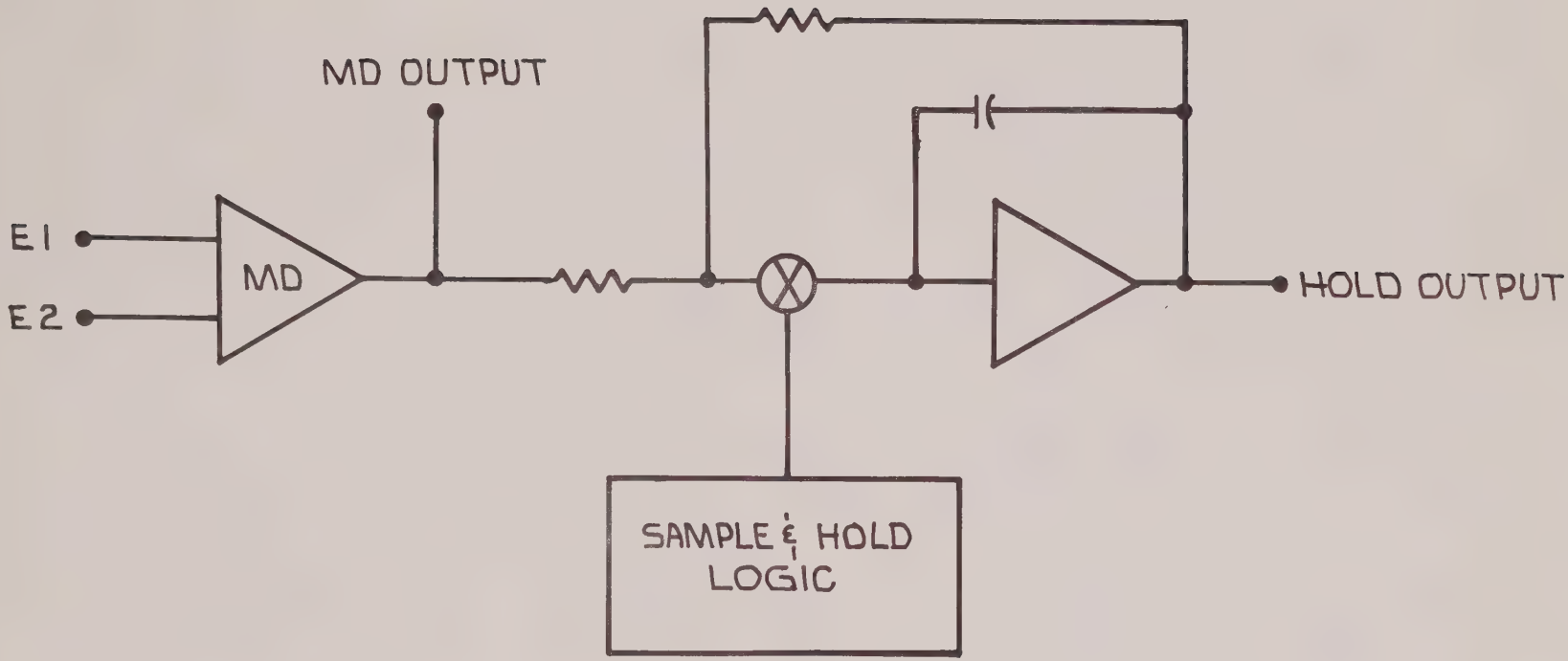
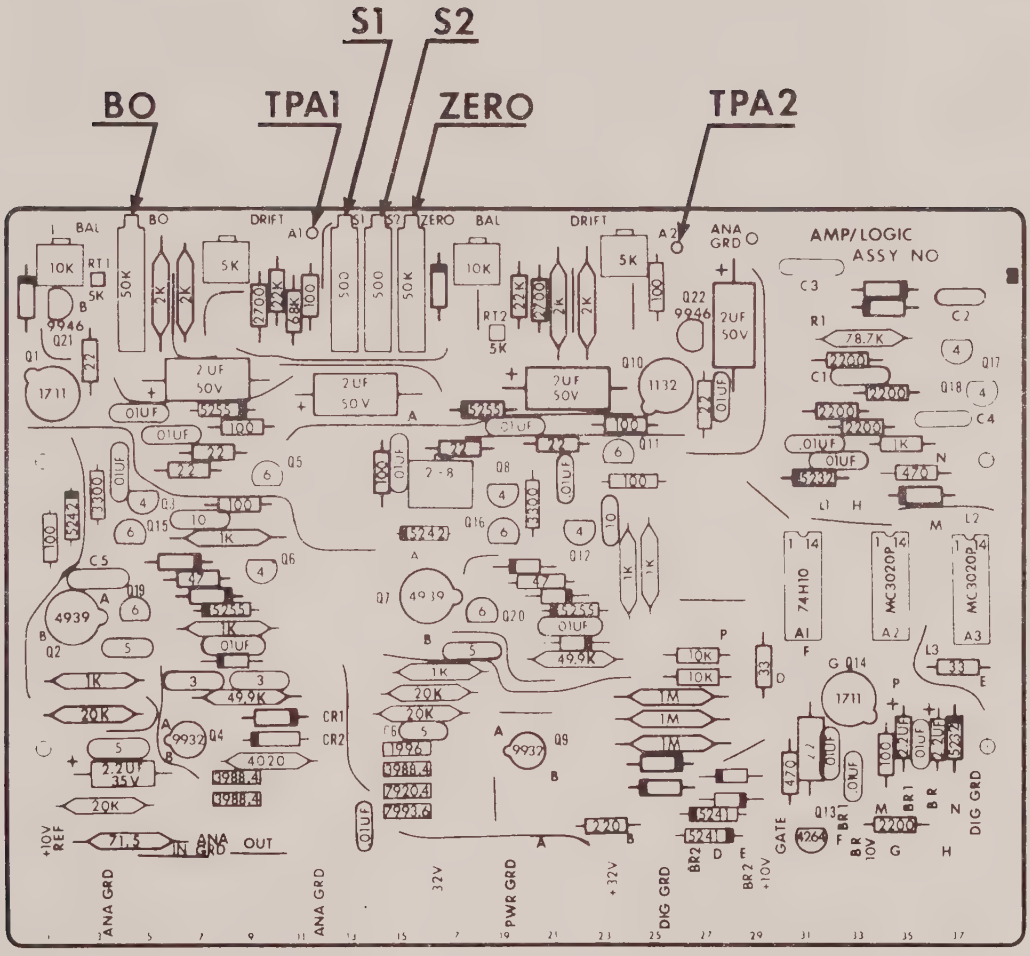


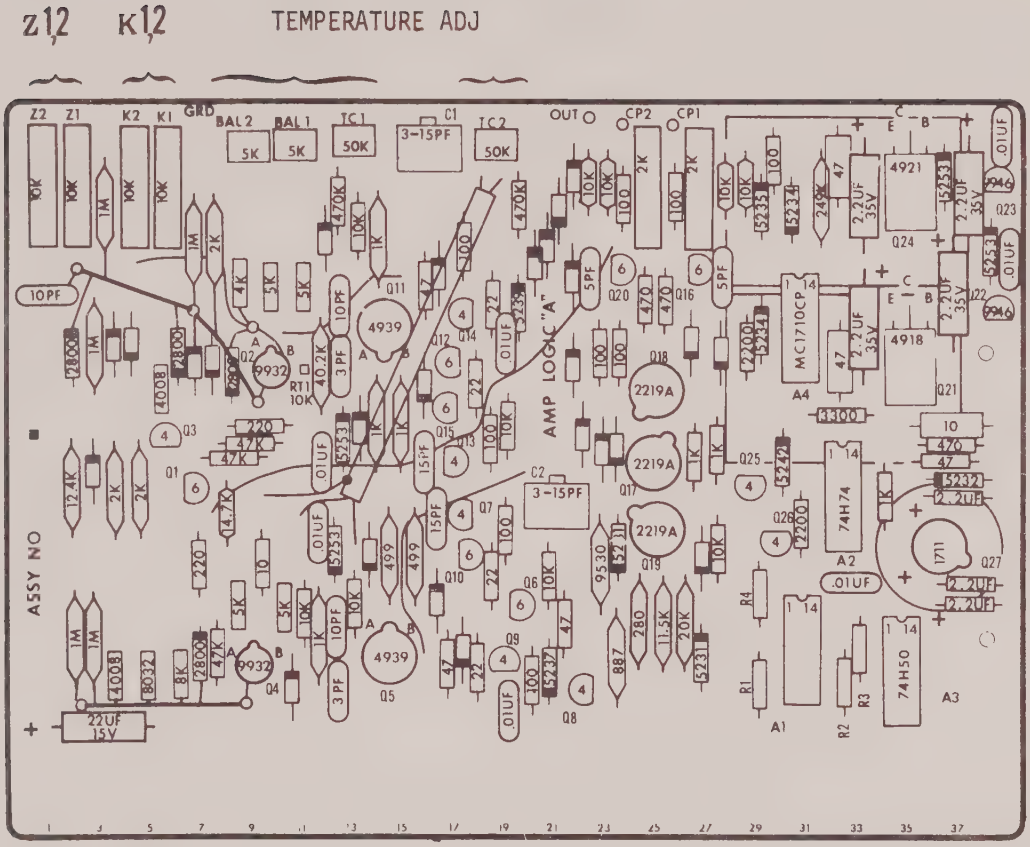
FIGURE 90016



POTENTIOMETER LOCATION

BIT BOARD - AB, B OR C

FIGURE 90017



POTENTIOMETER LOCATION

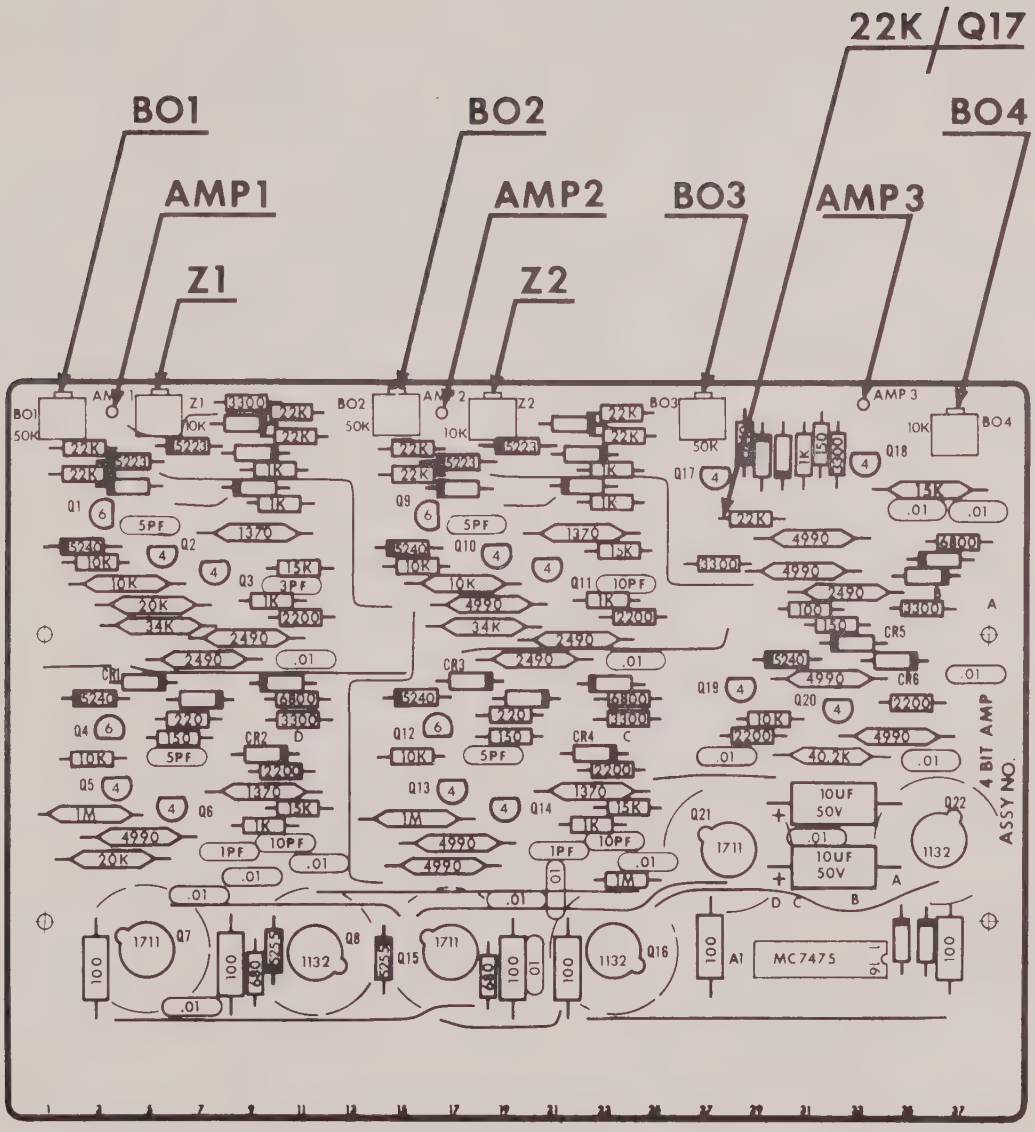
Bit Board "A"

FIGURE 90018

FRONT PANEL INDICATORS 8, 4, 2, 1	THEORETICAL INPUT (volts)	ACTUAL INPUT (volts)	ERROR
0000/0001	+8.75		
0001/0010	+7.5		
0010/0011	+6.25		
0011/0100	+5		
0100/0101	+3.75		
0101/0110	+2.5		
0110/0111	+1.25		
0111/1000	0		
1000/1001	-1.25		
1001/1010	-2.5		
1010/1011	-3.		
1011/1100	-5		
1100/1101	-6.25		
1101/1110	-7.5		
1110/1111	-8.75		

FOUR BIT LINEARITY

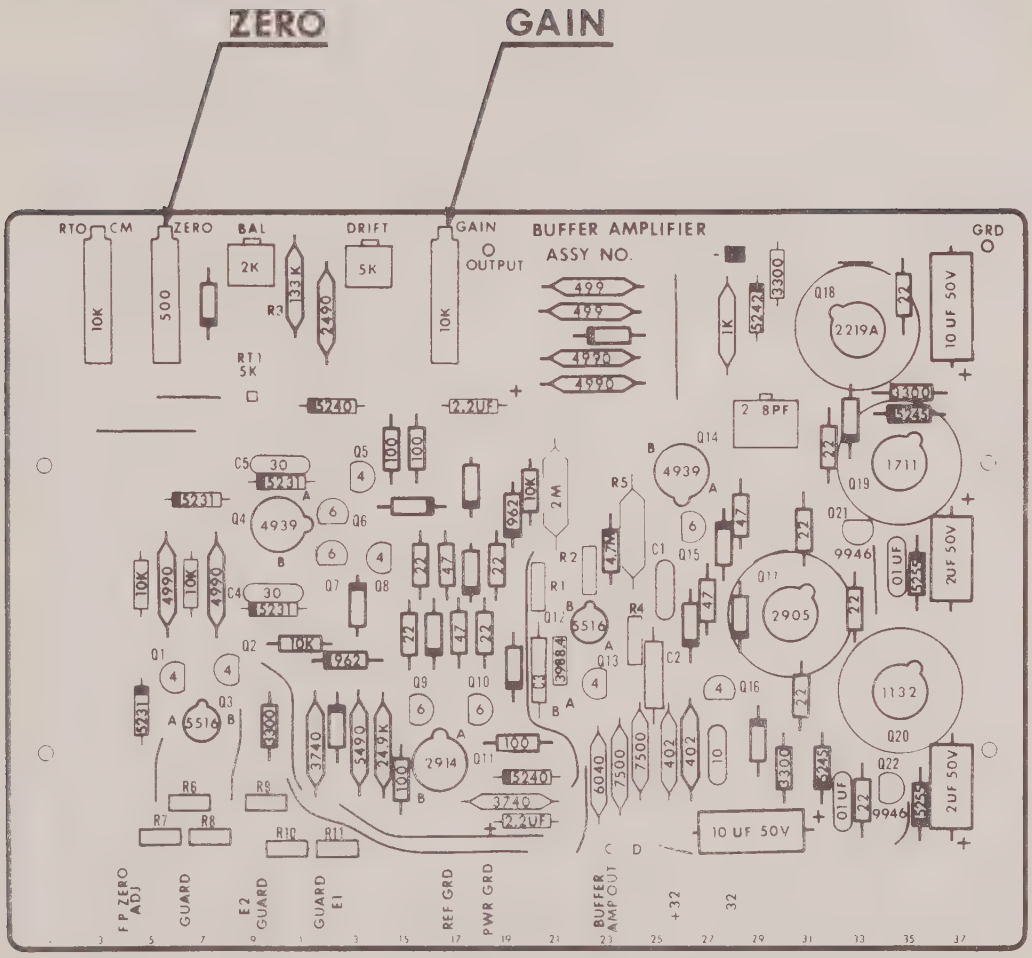
Figure 90019



POTENTIOMETER LOCATION

4-BIT AMPLIFIER

FIGURE 90020



POTENTIOMETER LOCATION

BUFFER AMPLIFIER

FIGURE 90021

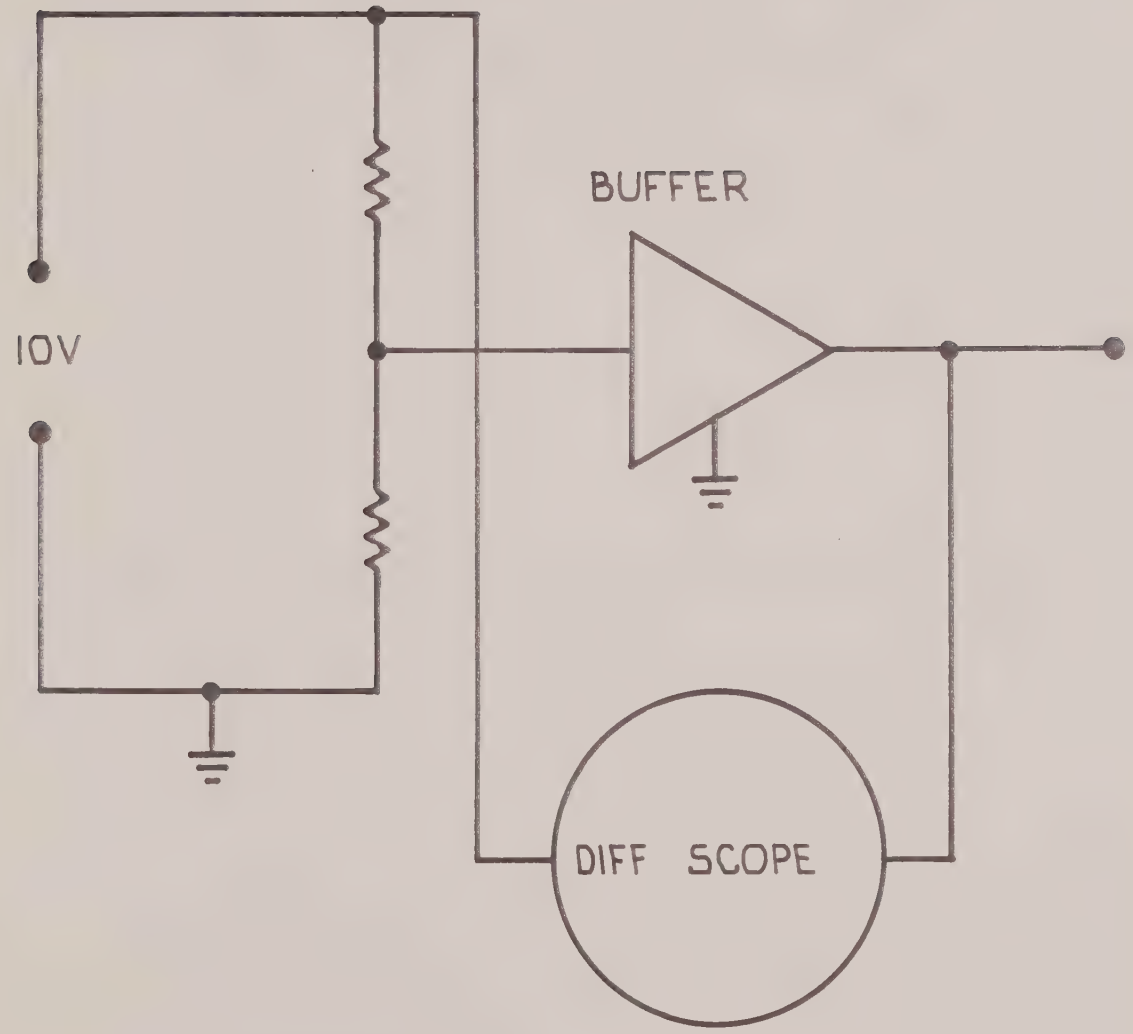


FIGURE 90022

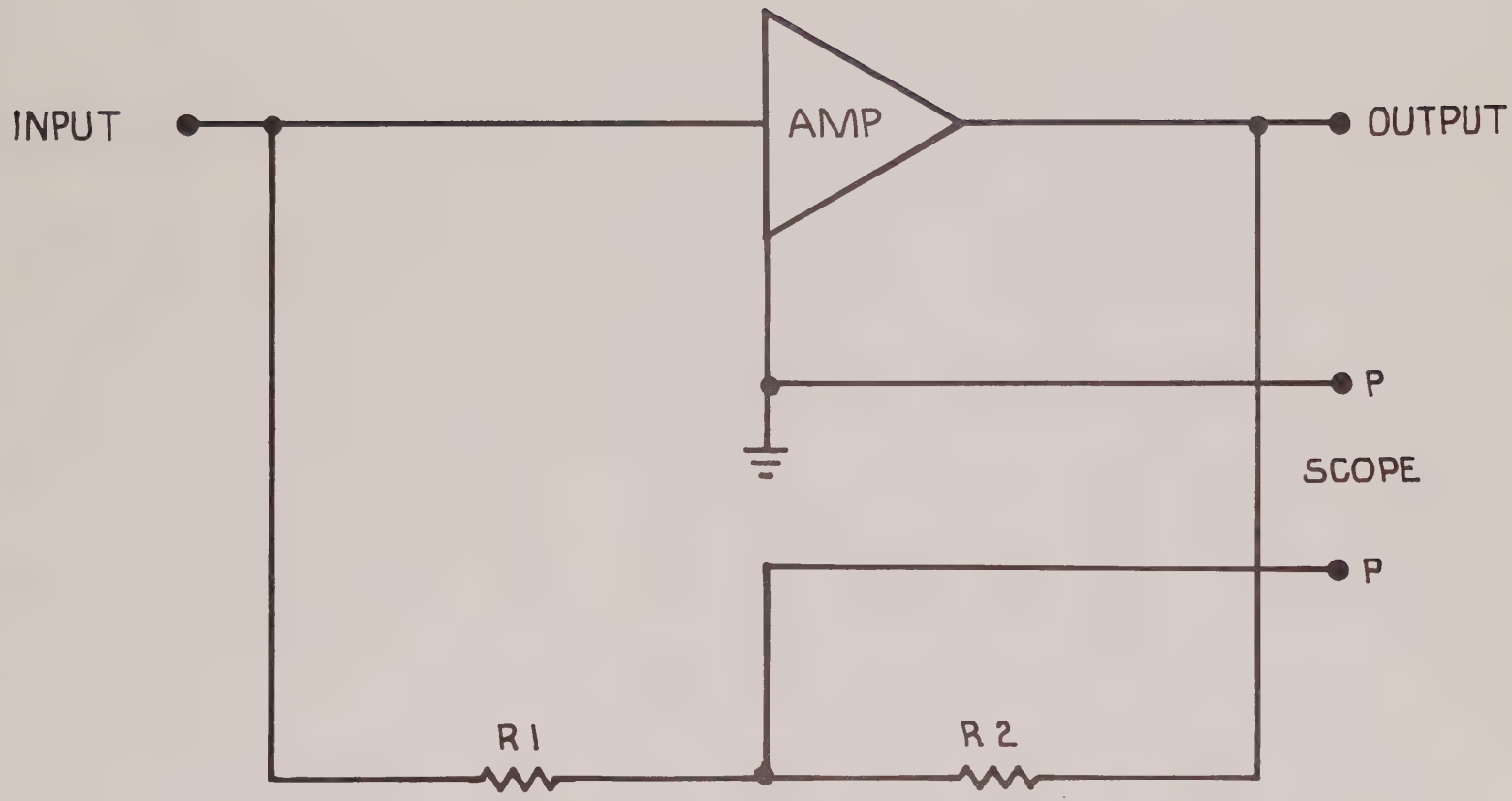
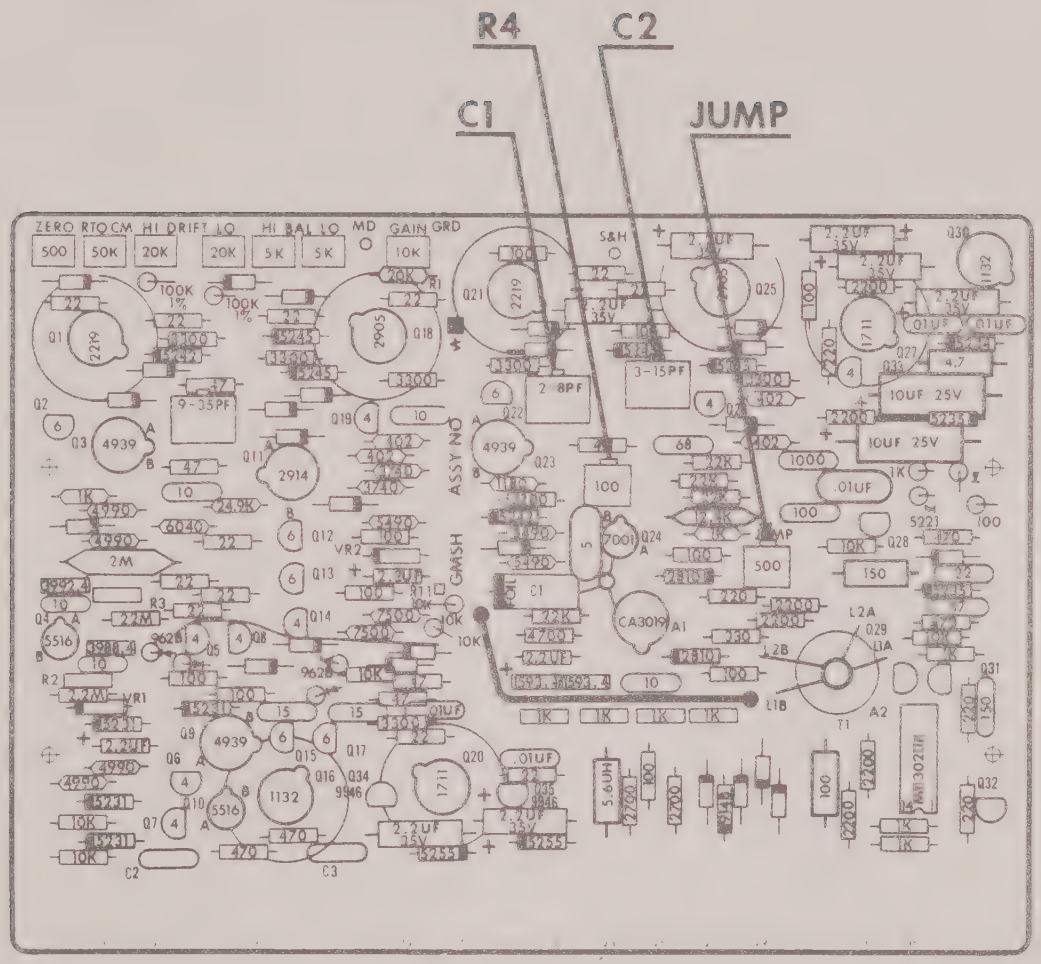


FIGURE 90023



SAMPLE-AND-HOLD AMPLIFIER

FIGURE 90024

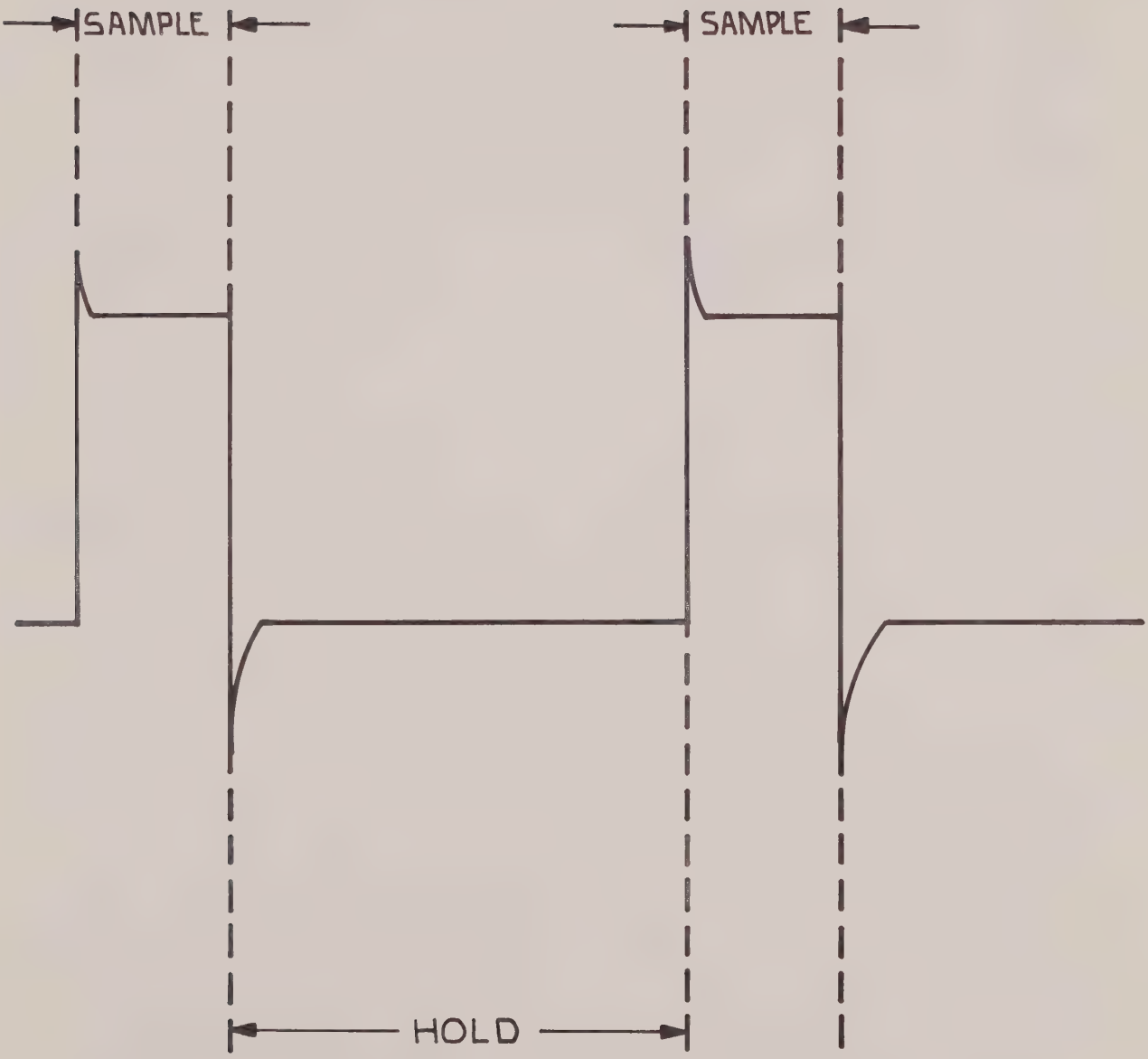


FIGURE 90025

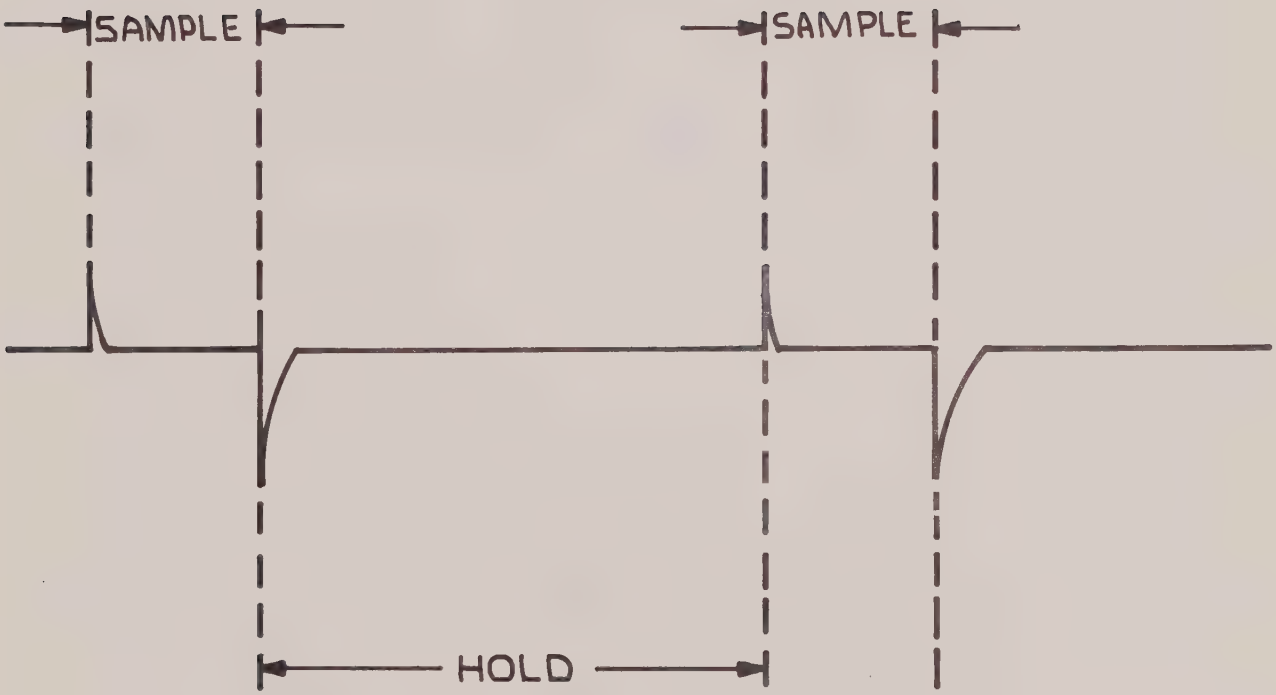
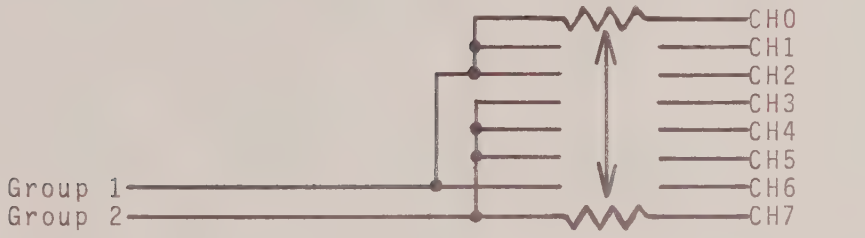


FIGURE 90026

SINGLE-ENDED INPUTS

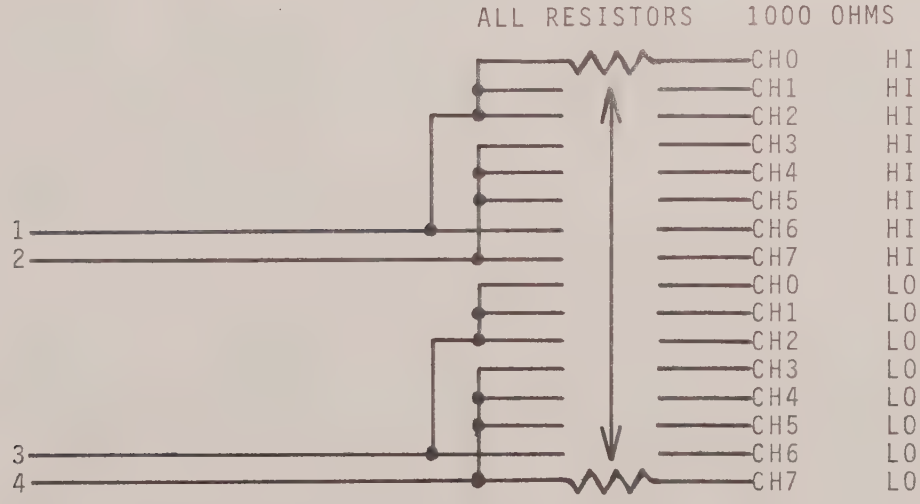
FIGURE 90027



Lo inputs tied to analog gnd. If more channels are present than 8 this same pattern is repeated.

DIFFERENTIAL INPUTS

FIGURE 90028



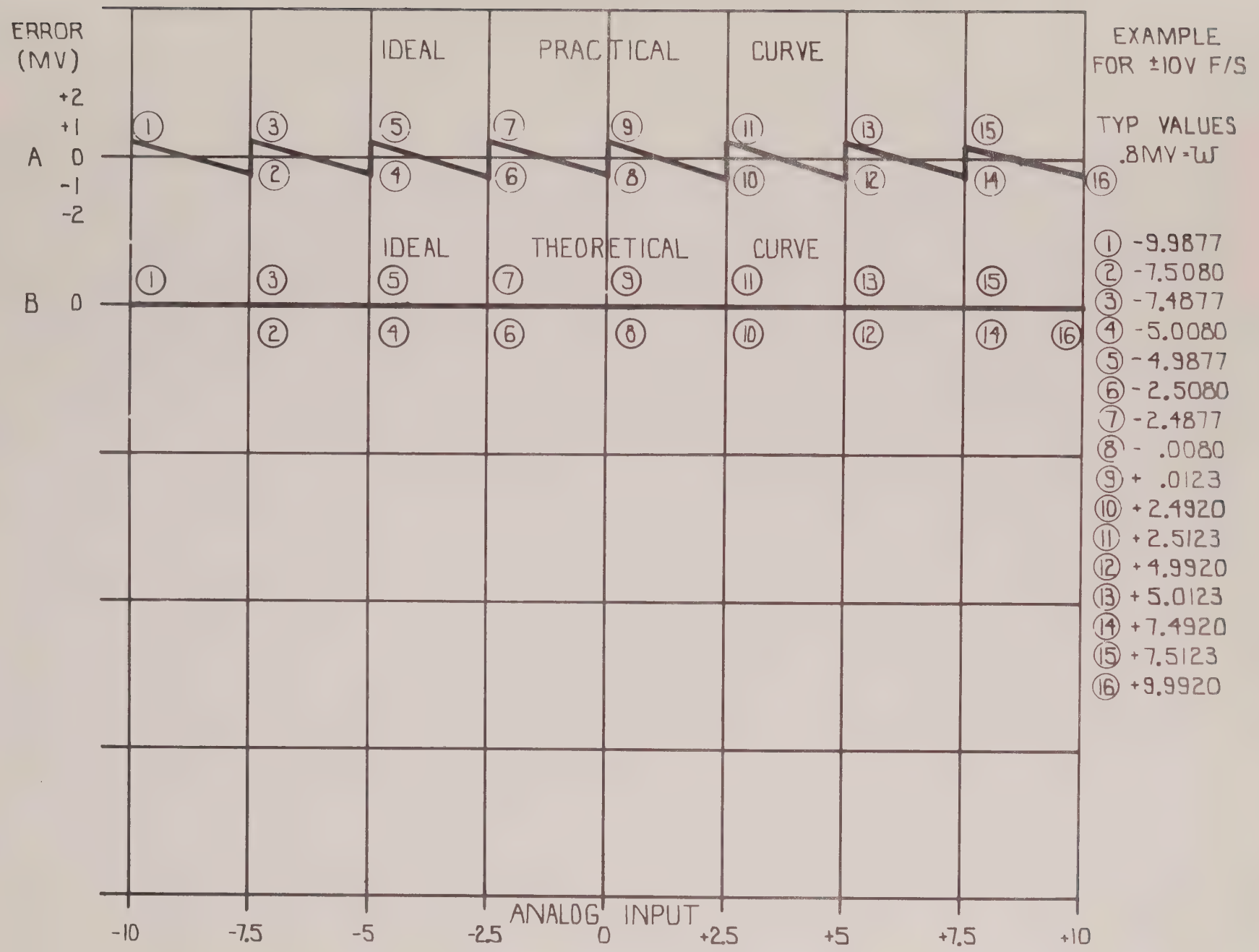


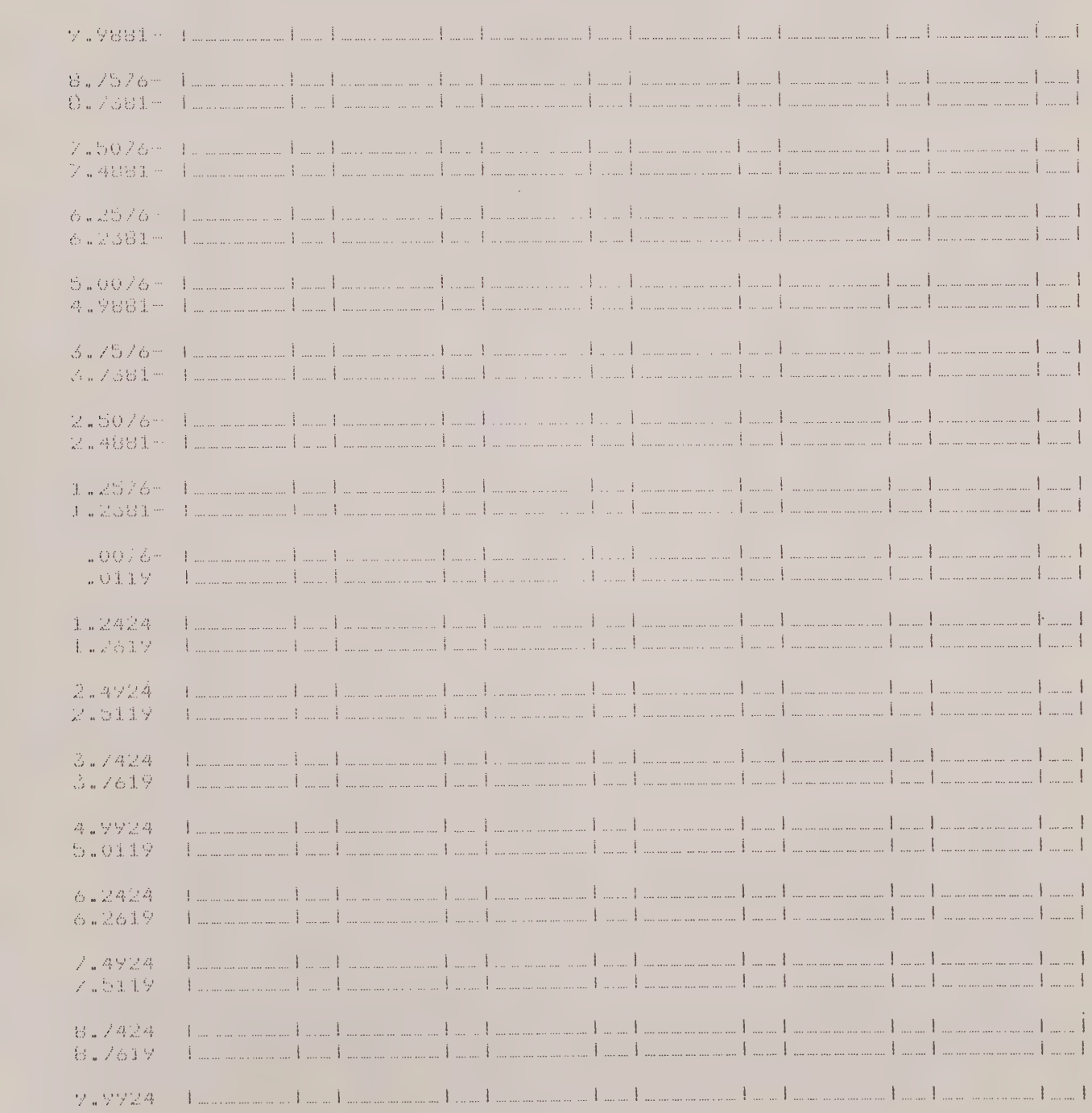
FIGURE 90029

FIGURE 90030

PART NU._____ SERIAL NO._____

NU. OF BITS= 14(PLUS THE SIGN BIT) FULL SCALE VOLTAGE= 10.0000

MILLIVOLTS PER COUNT= .6103



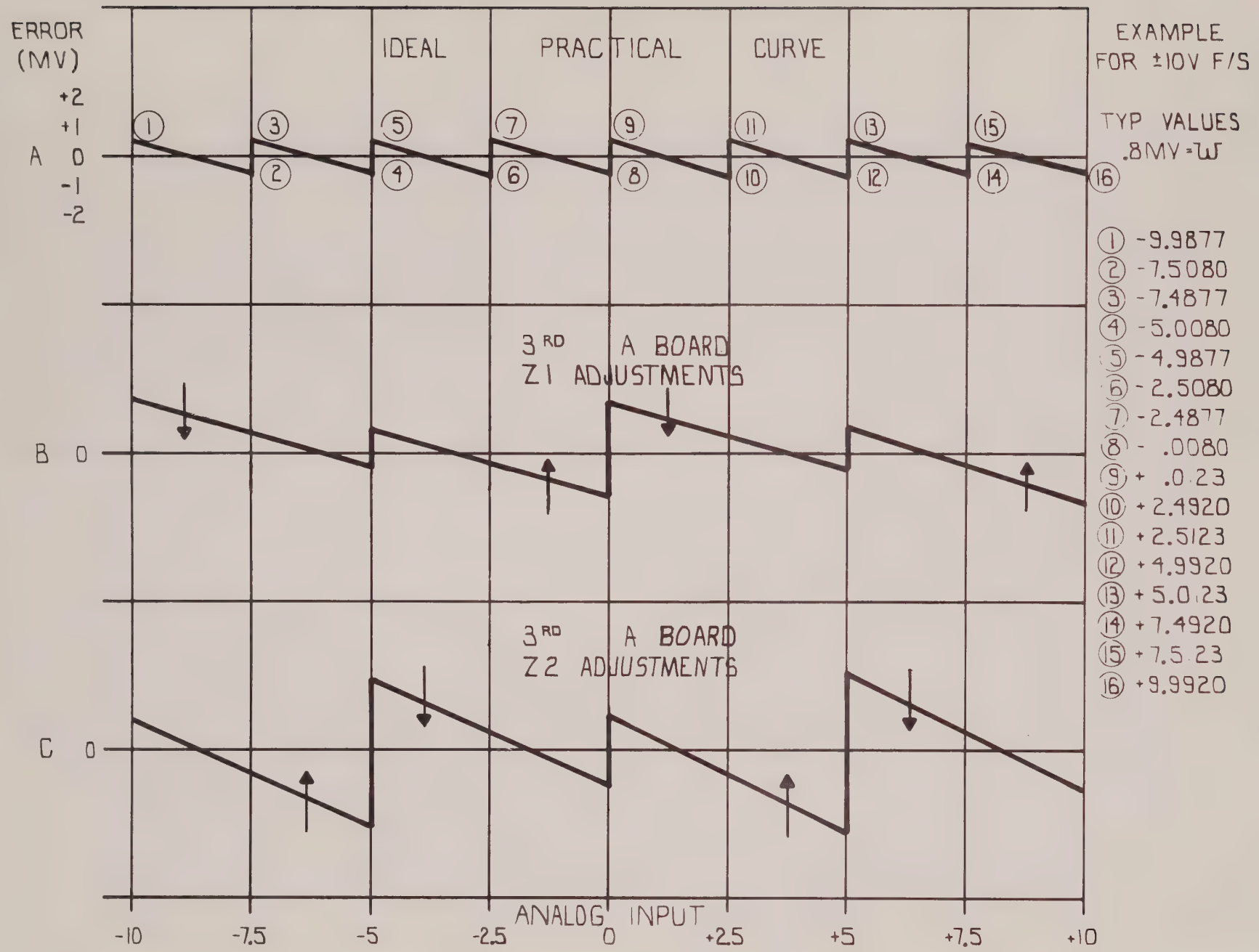


FIGURE 90031

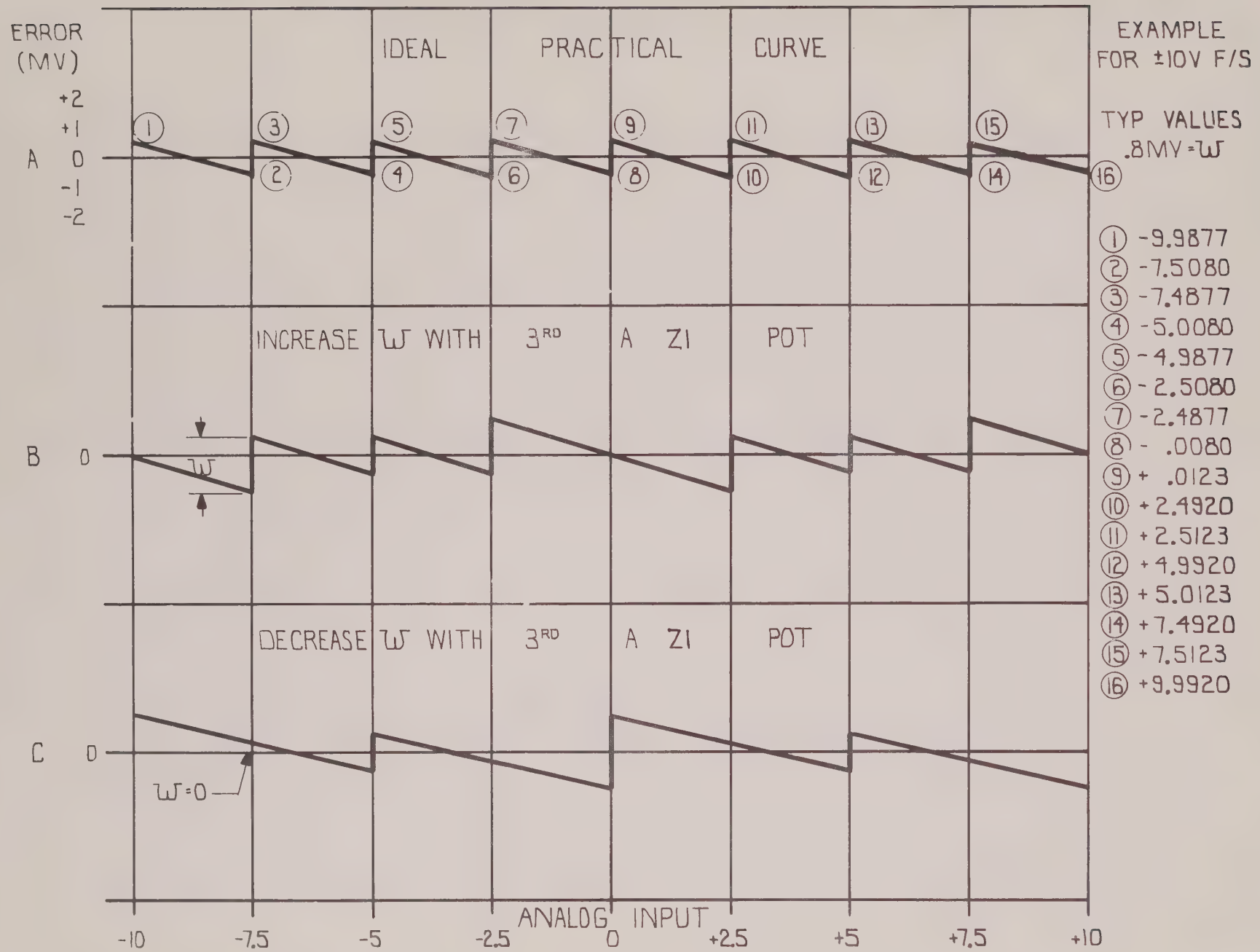


FIGURE 90032

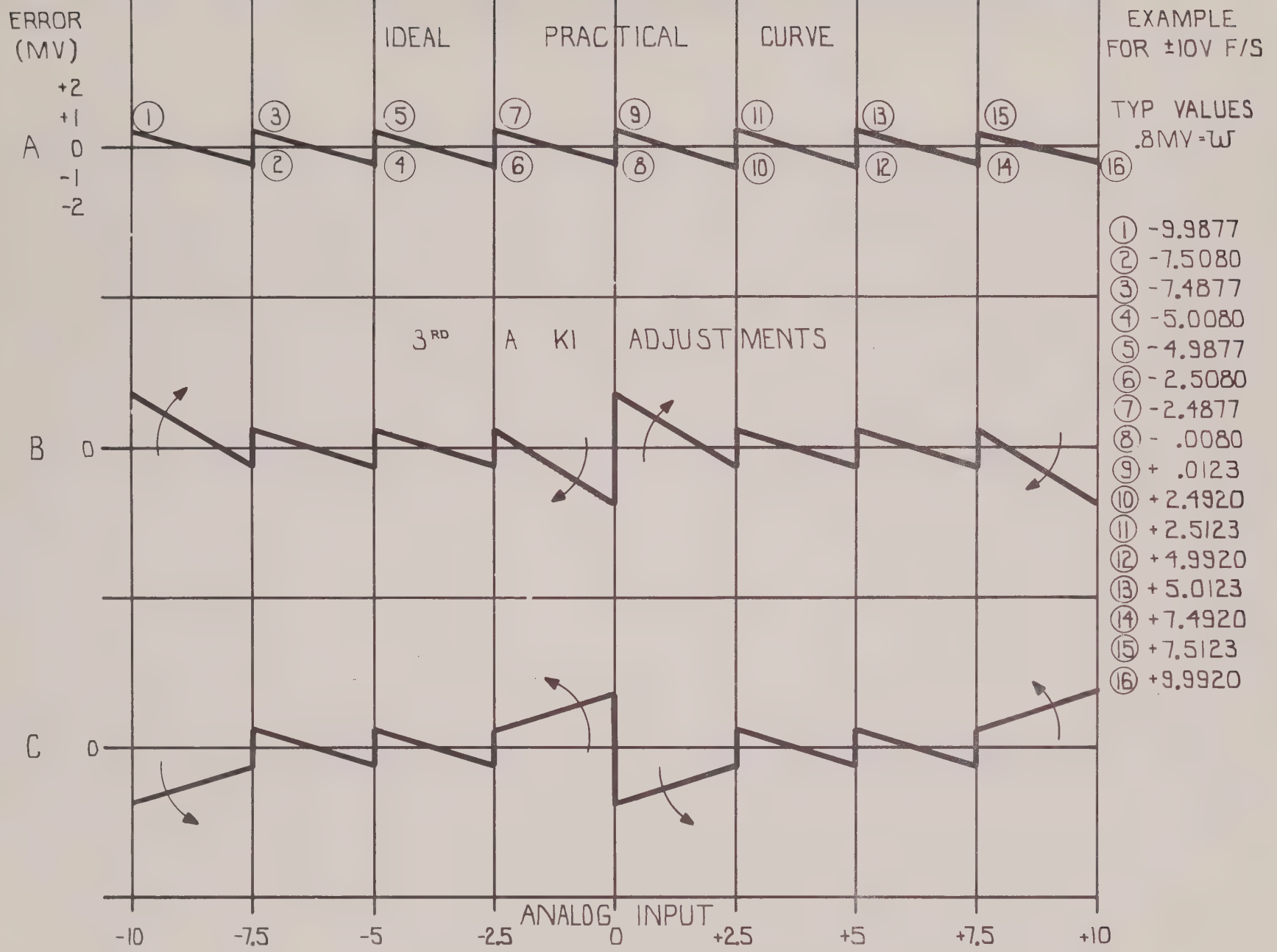


FIGURE 90033

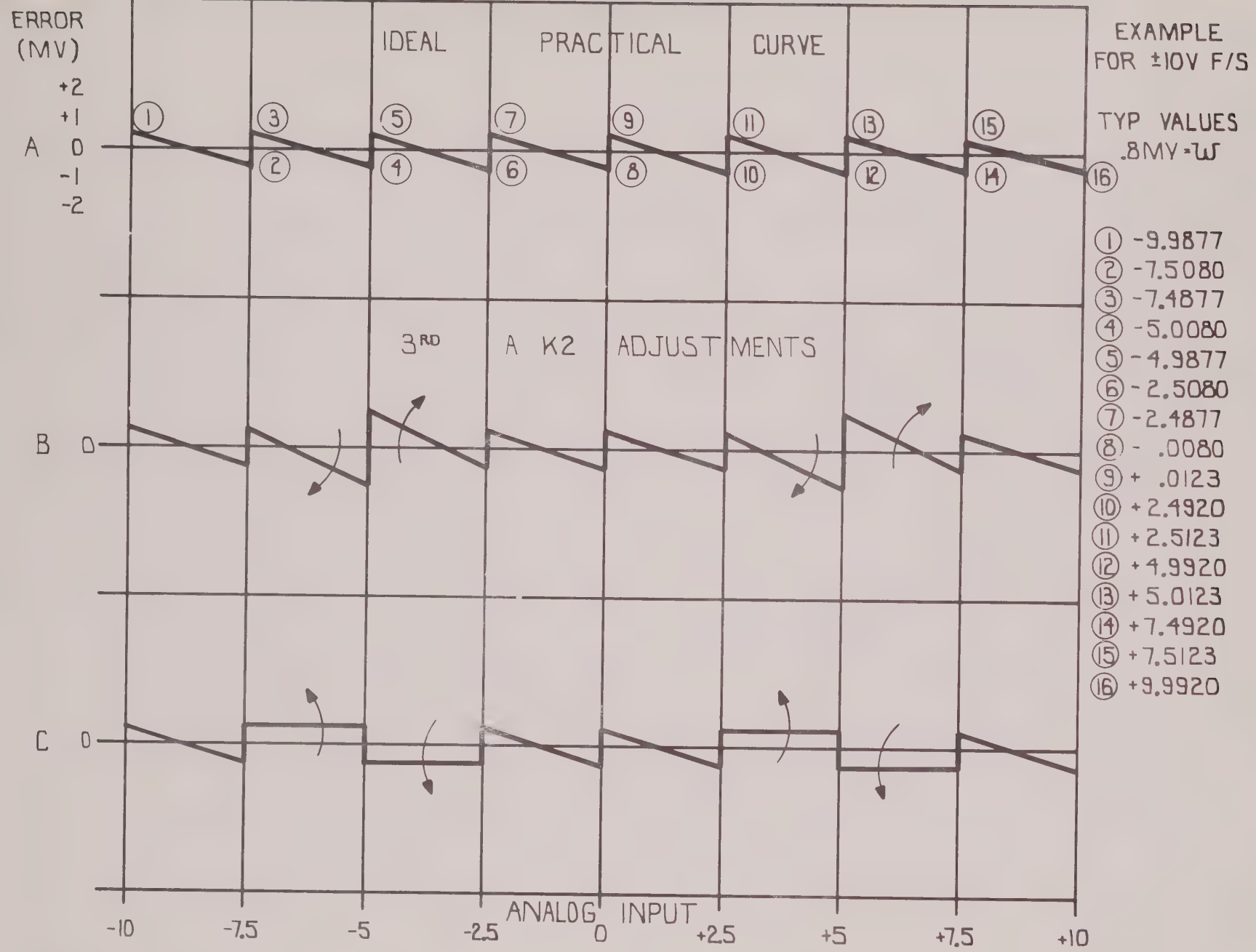


FIGURE 90034

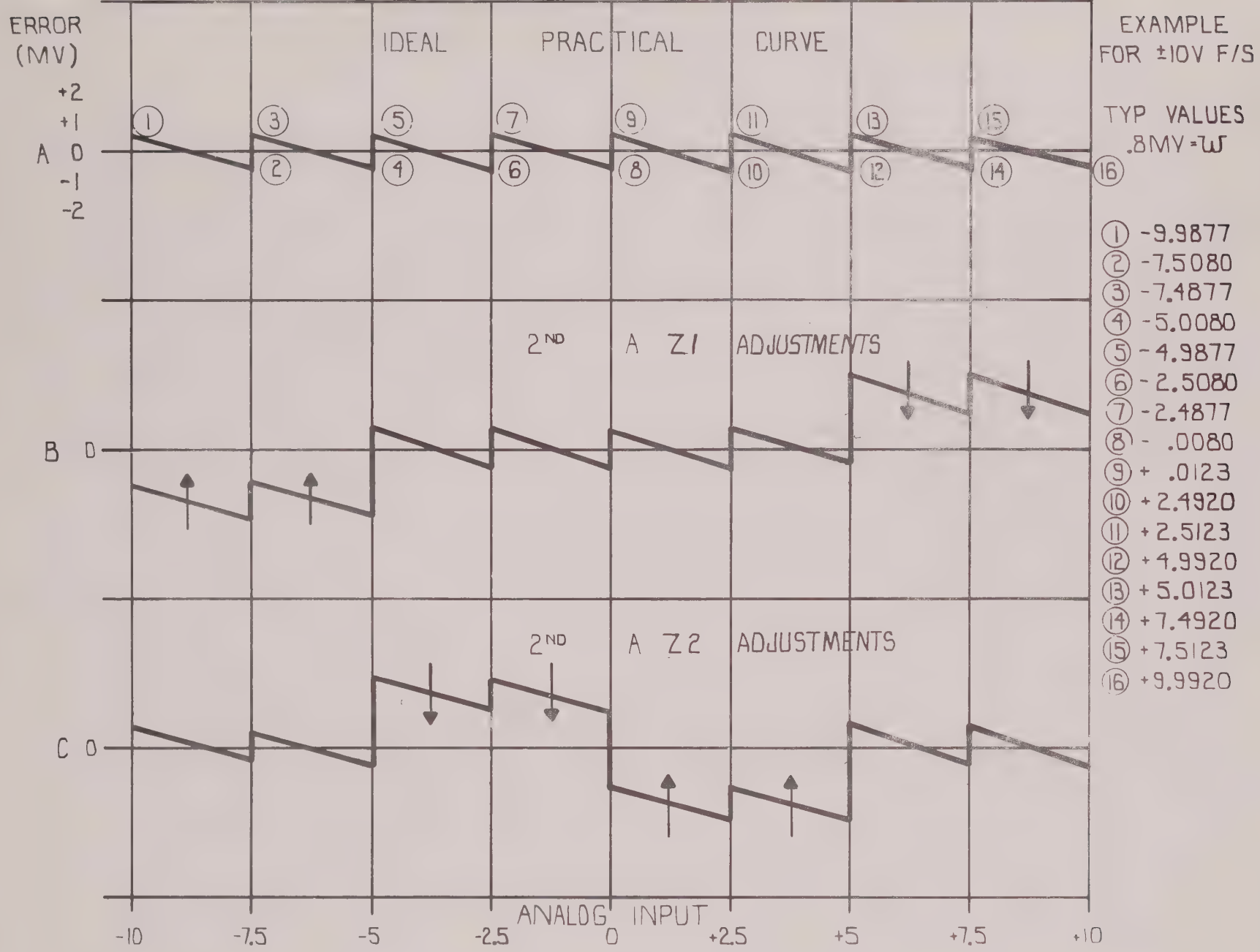


FIGURE 90035

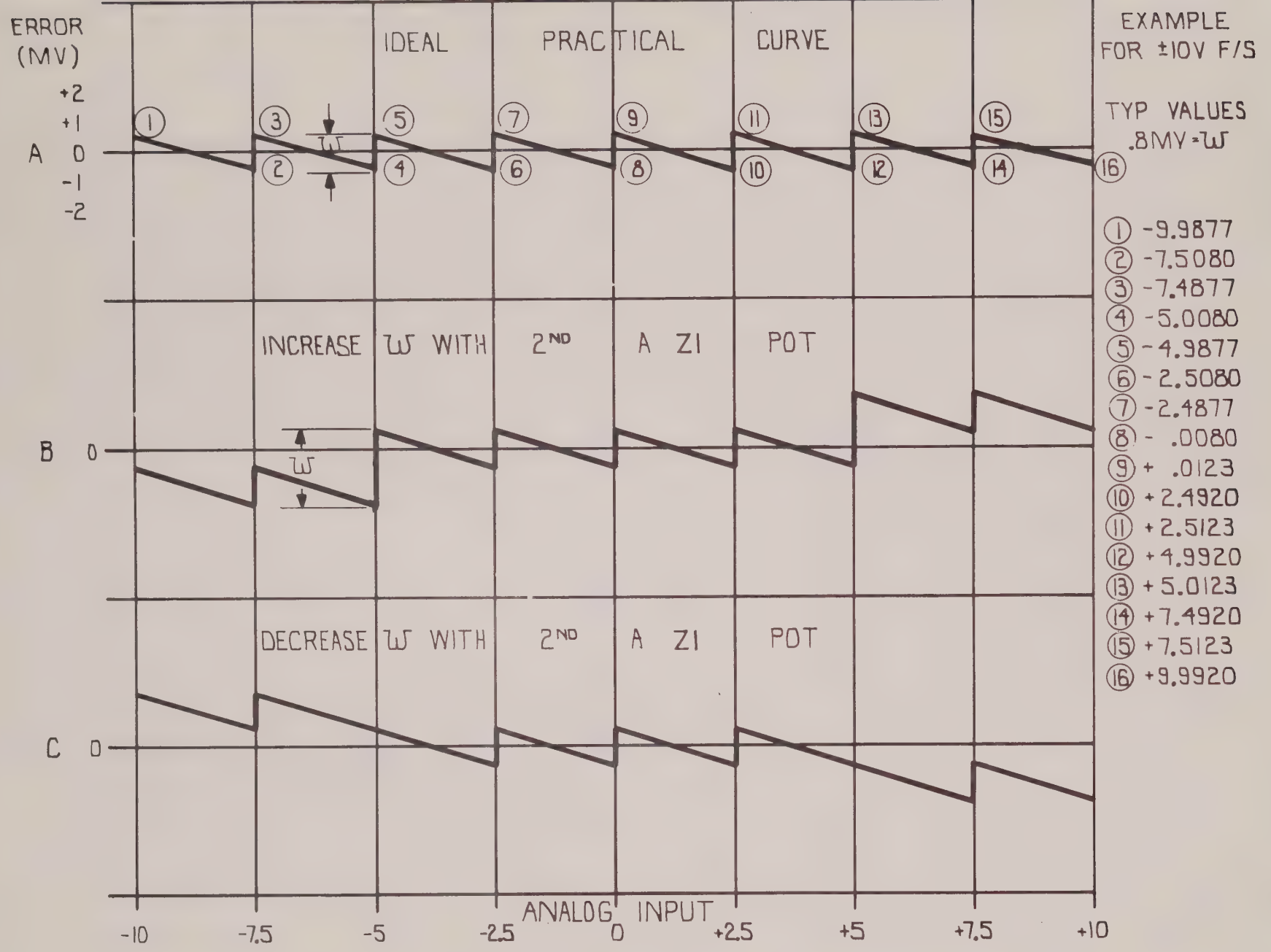


FIGURE 90036

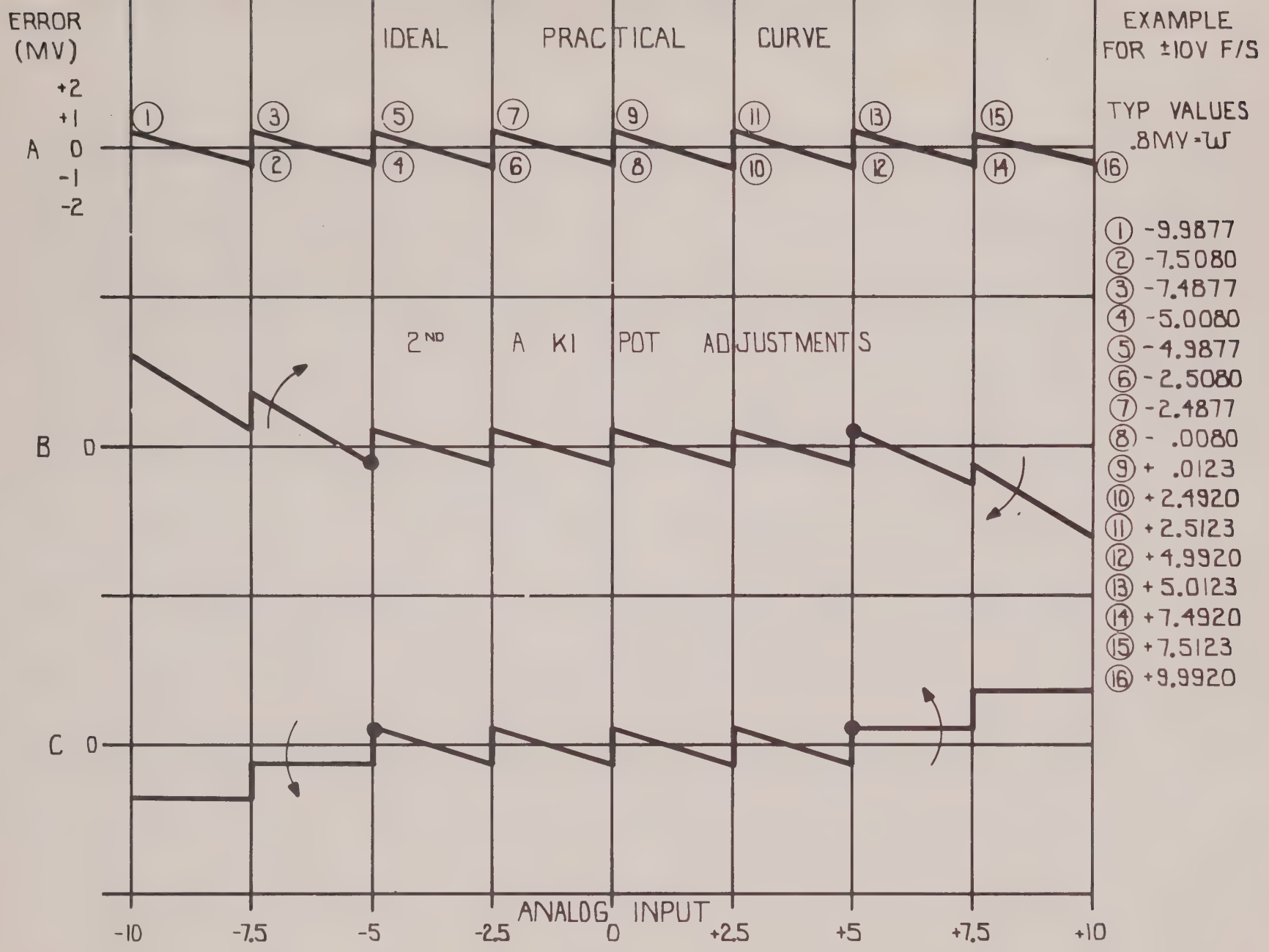


FIGURE 90037

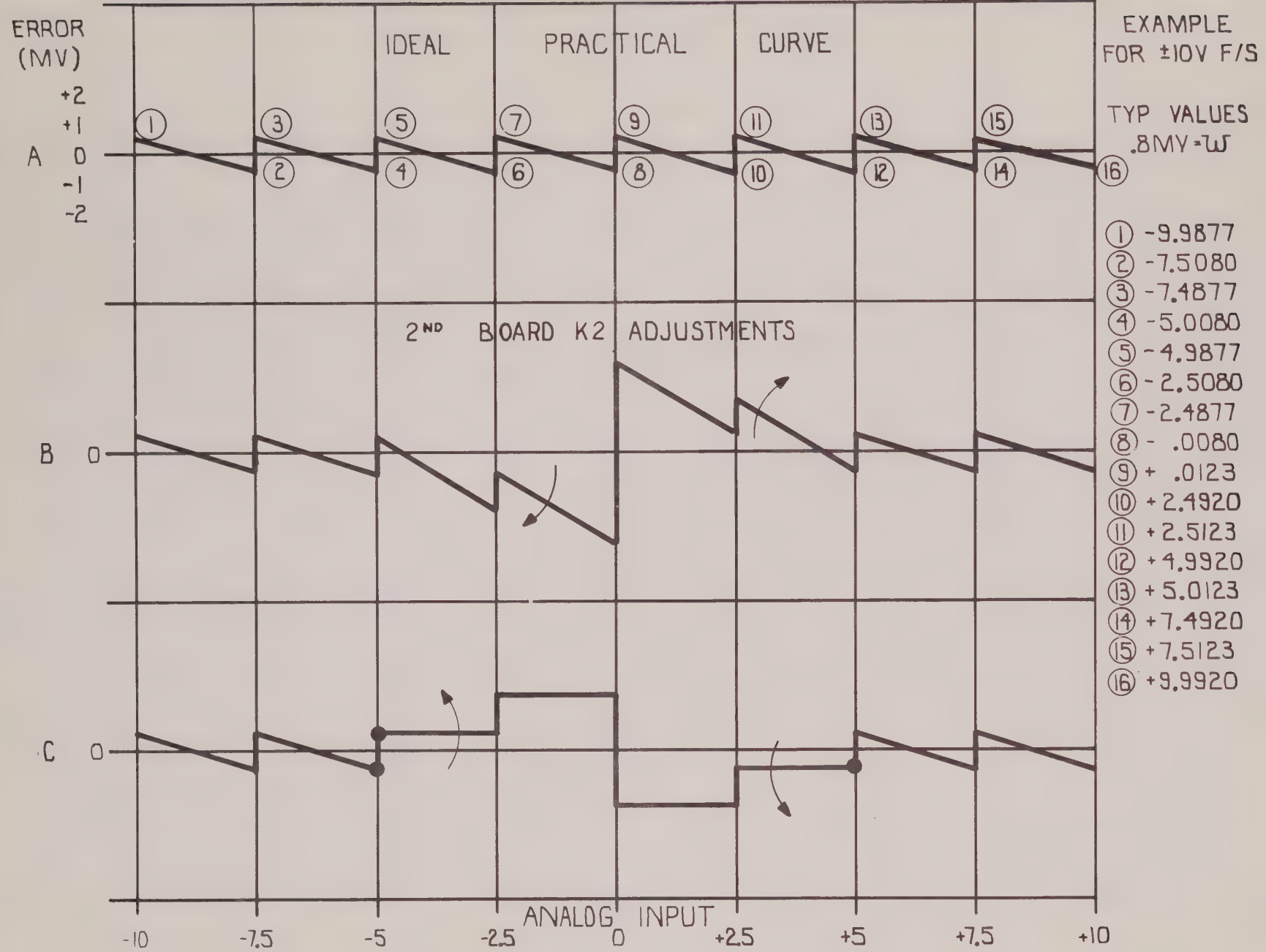


FIGURE 90038

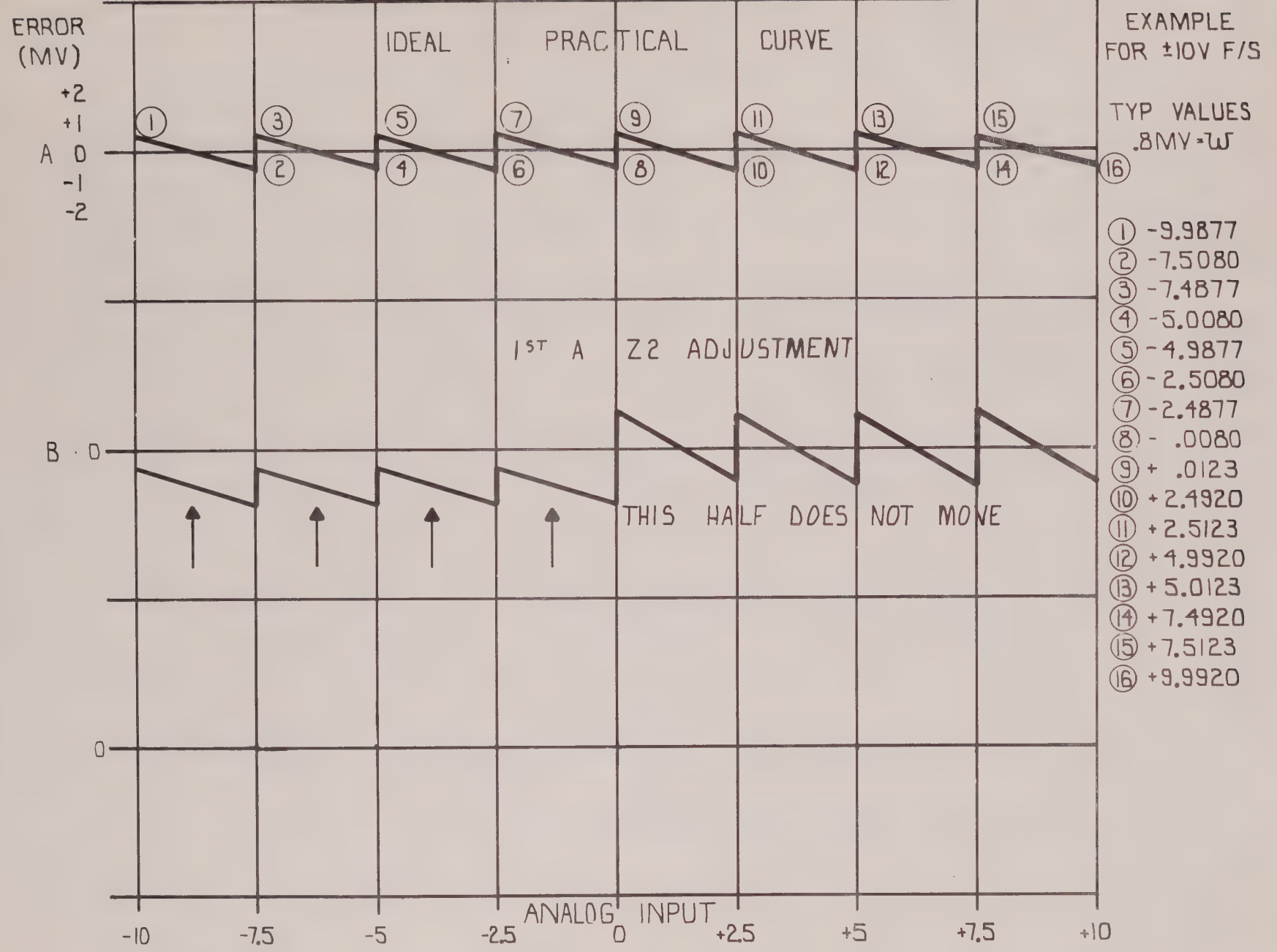


FIGURE 90039

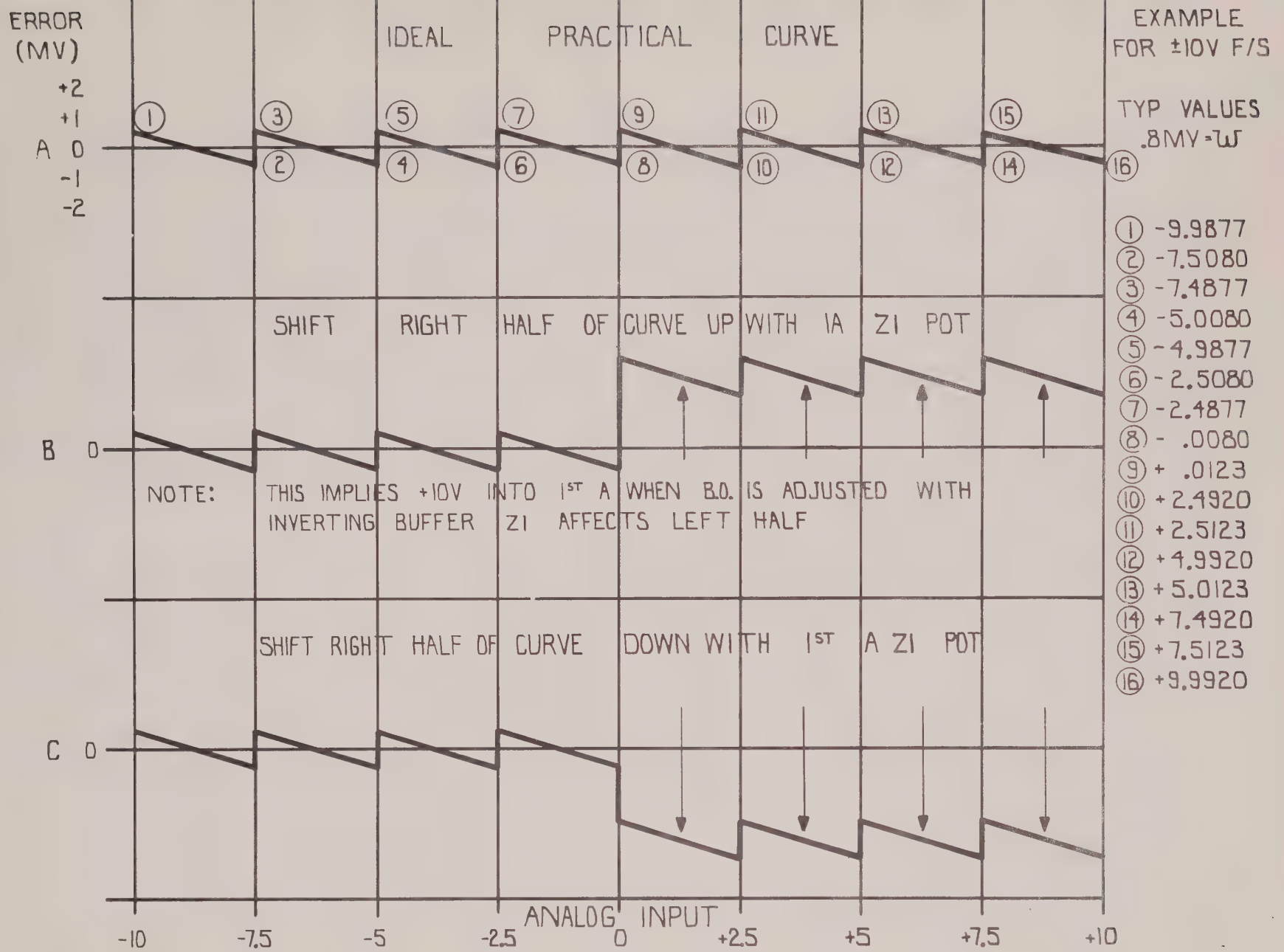


FIGURE 90040

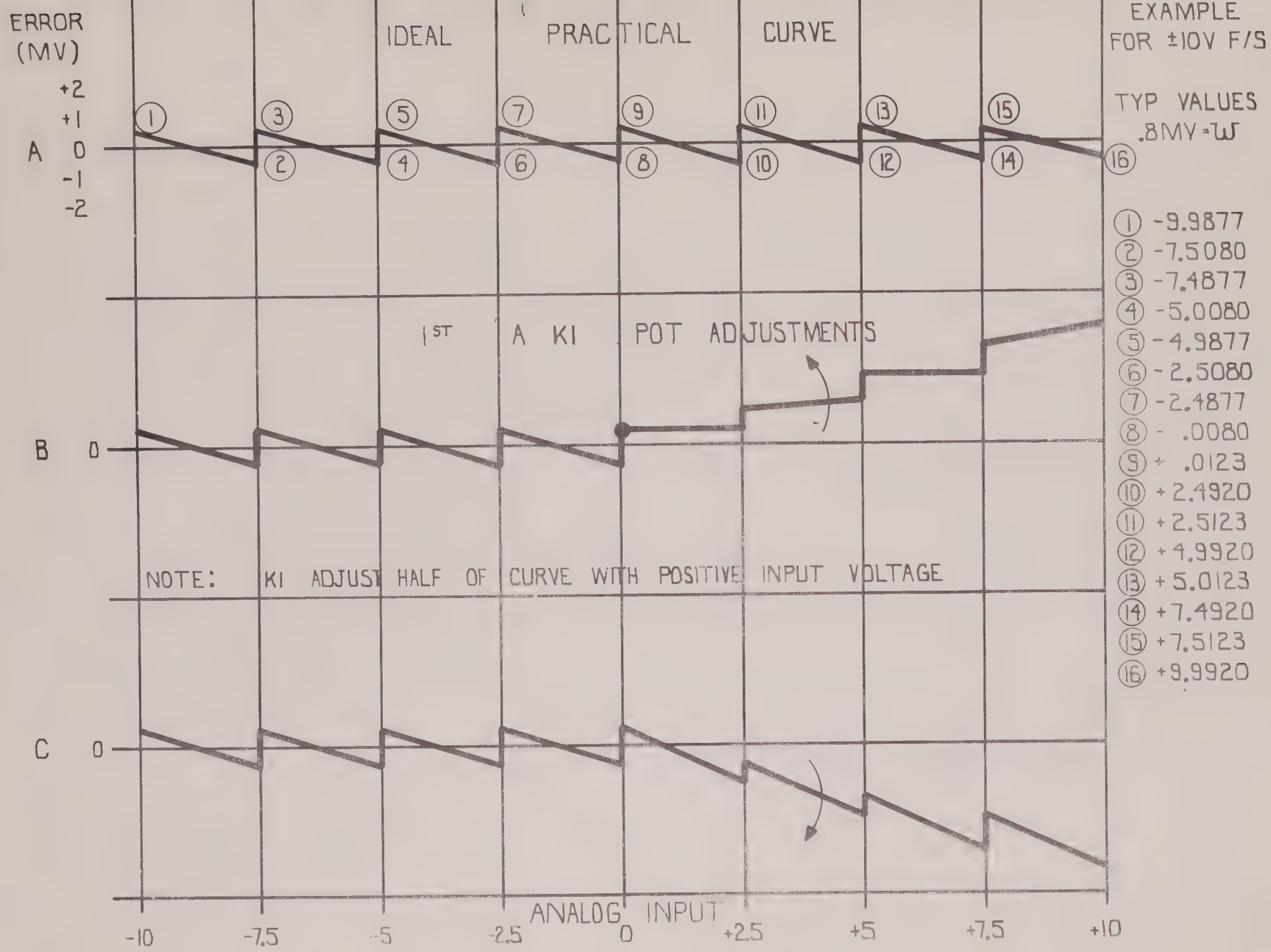


FIGURE 90041

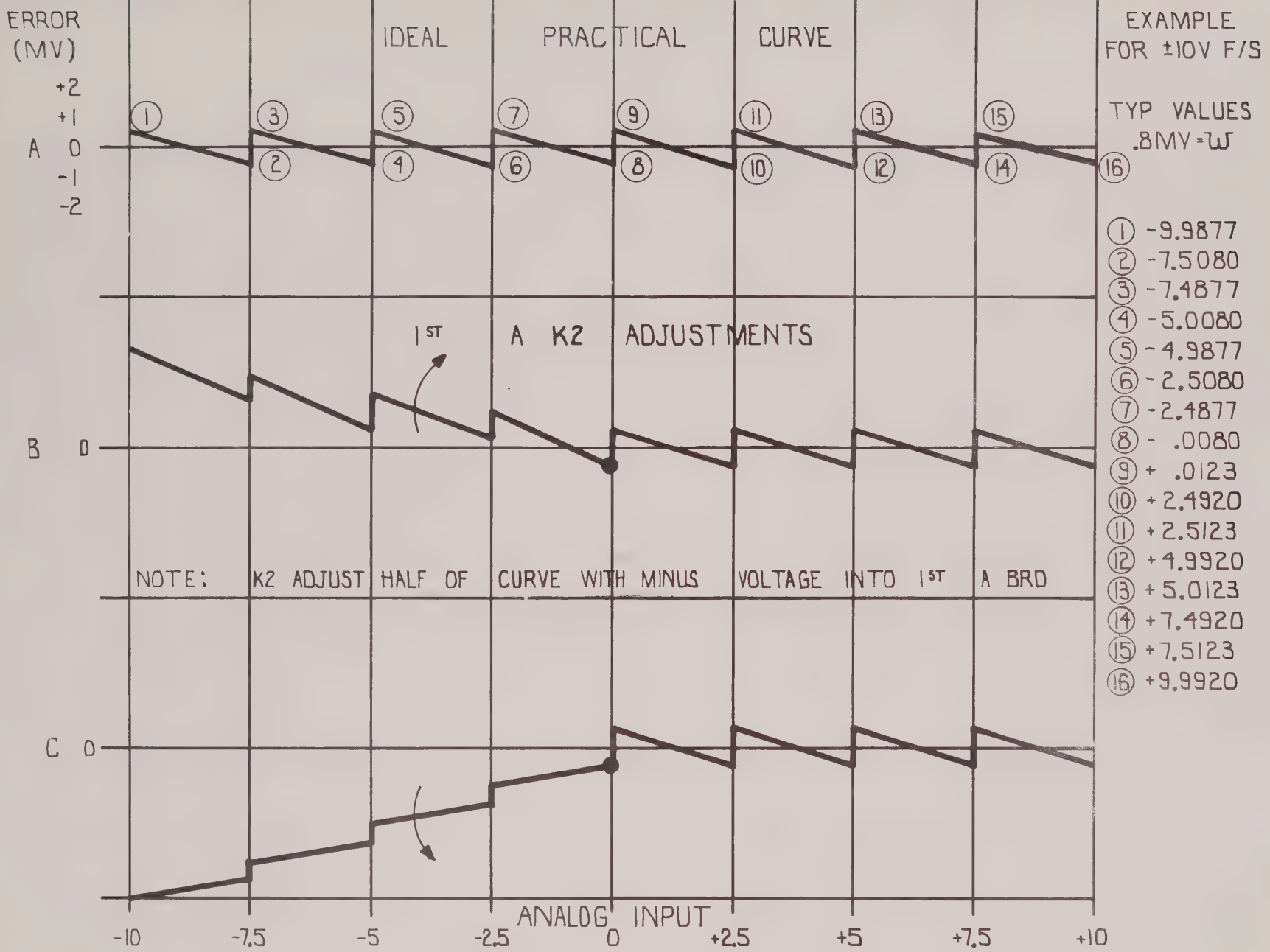


FIGURE 90042

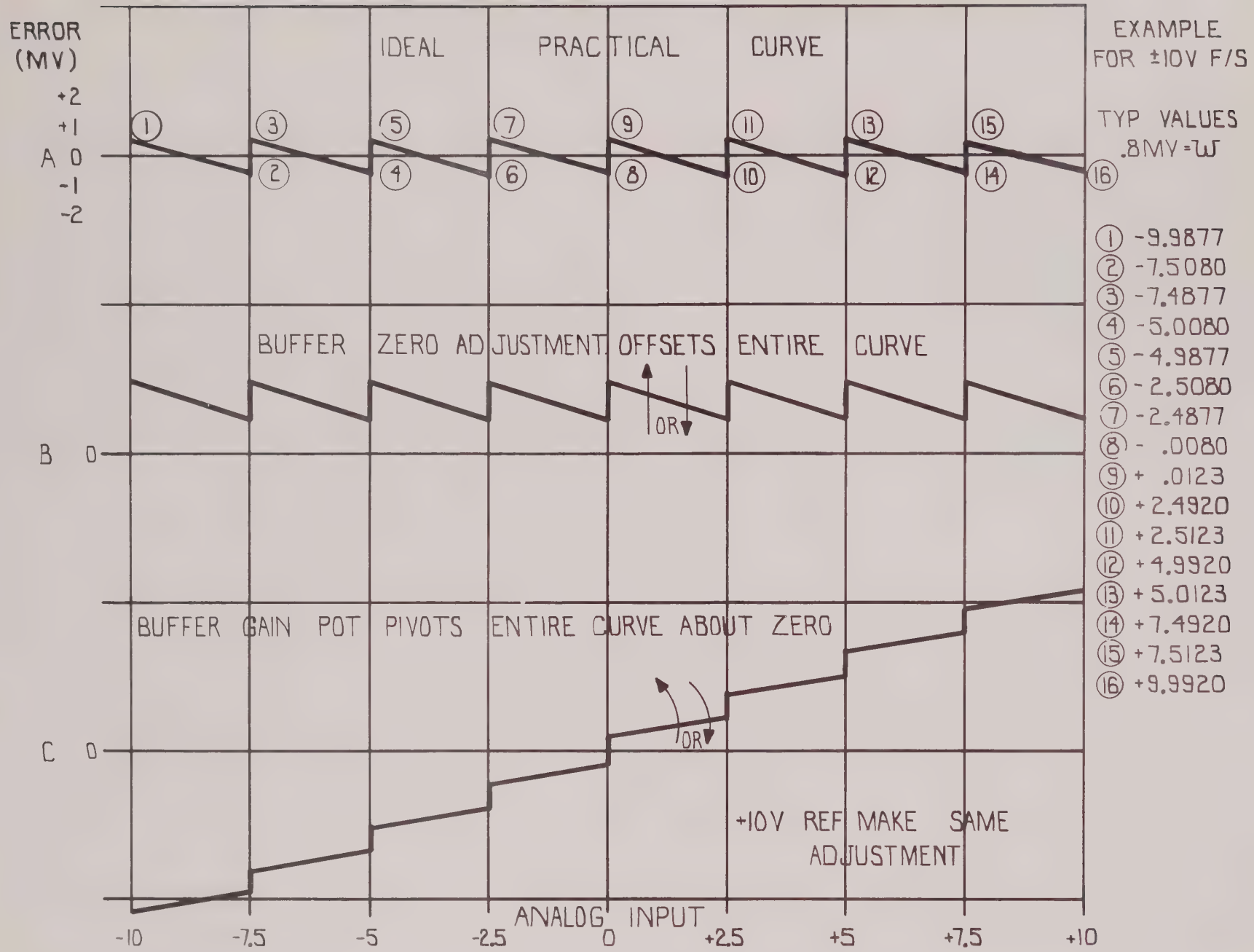


FIGURE 90043

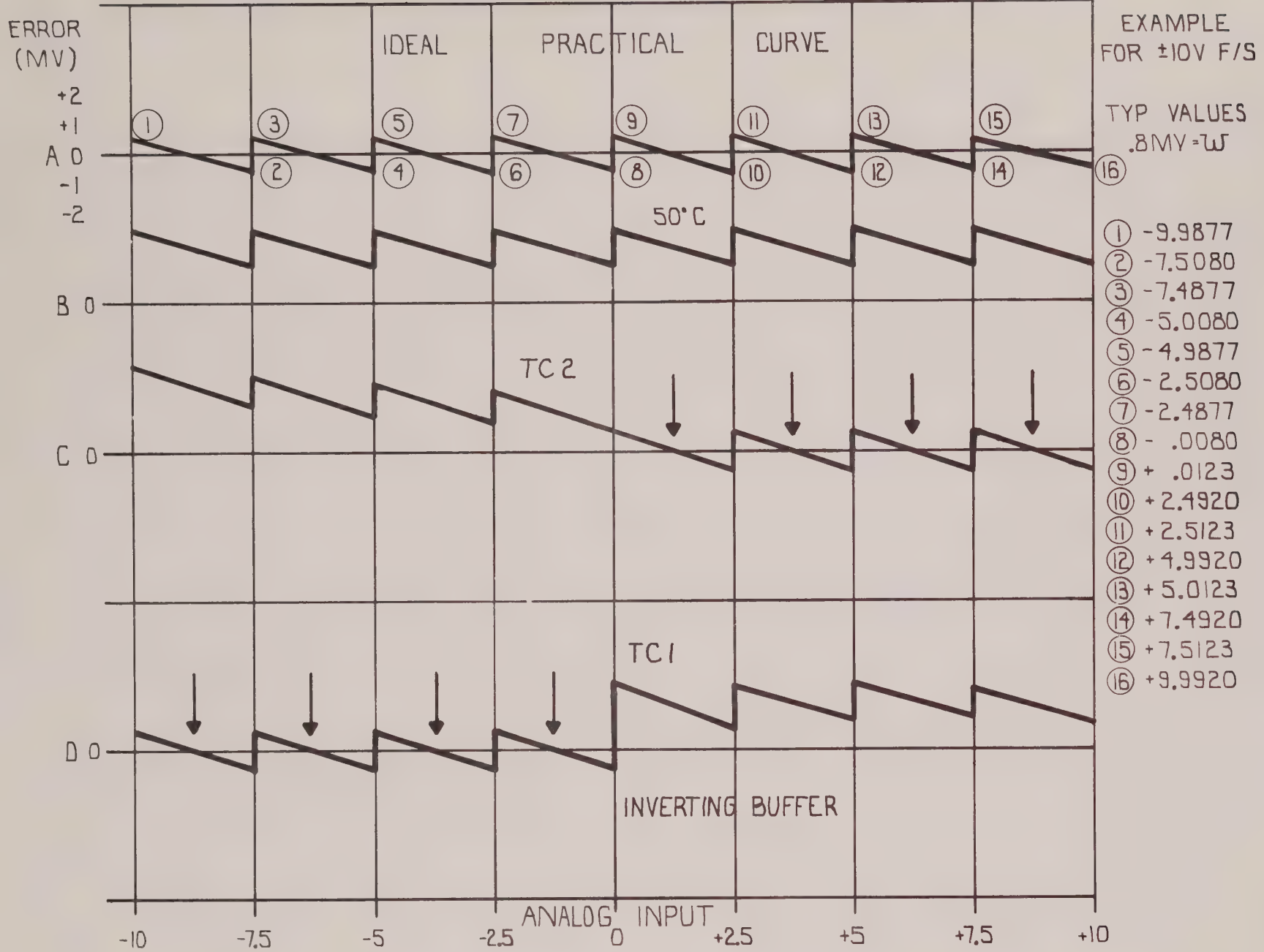


FIGURE 90044

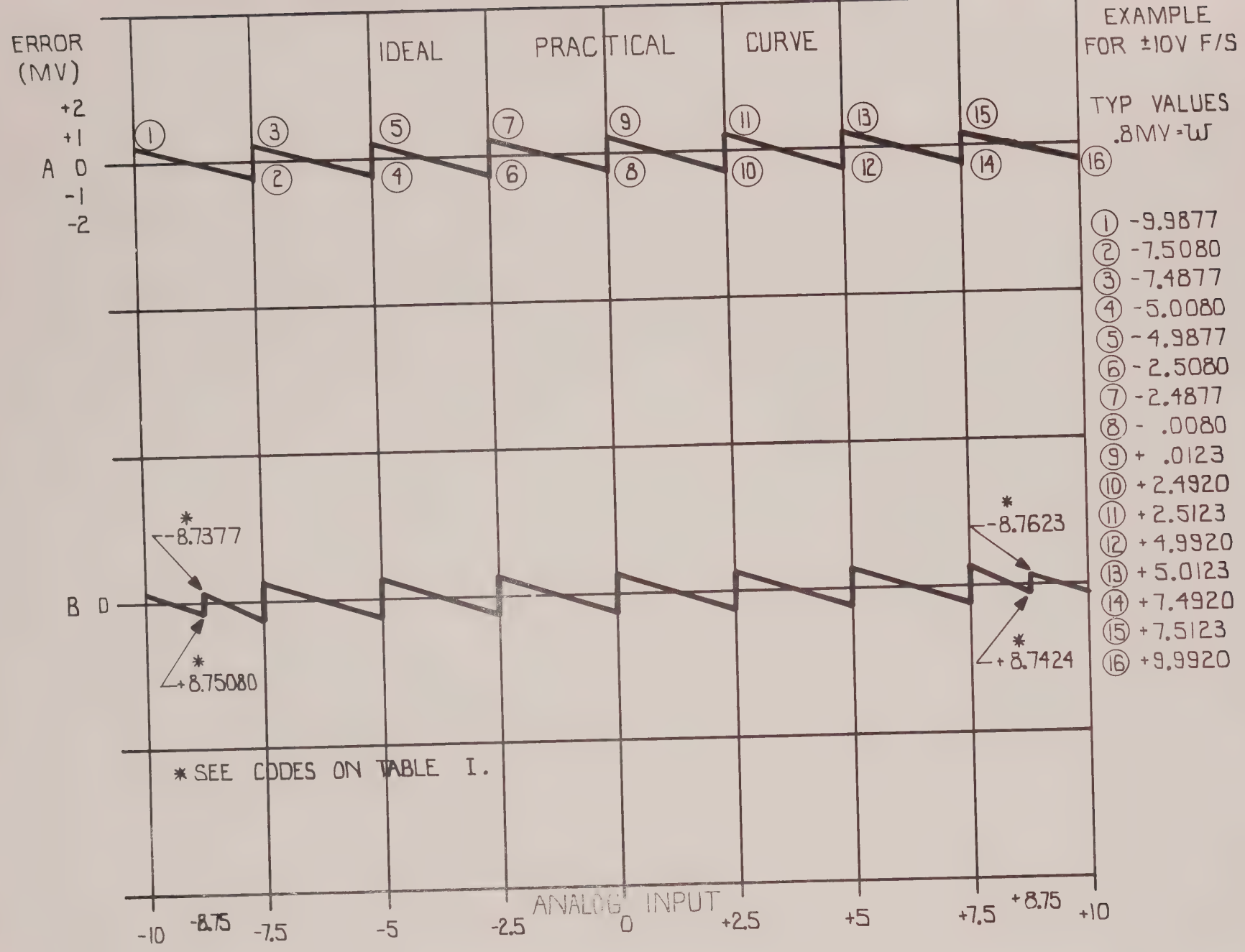


FIGURE 90045

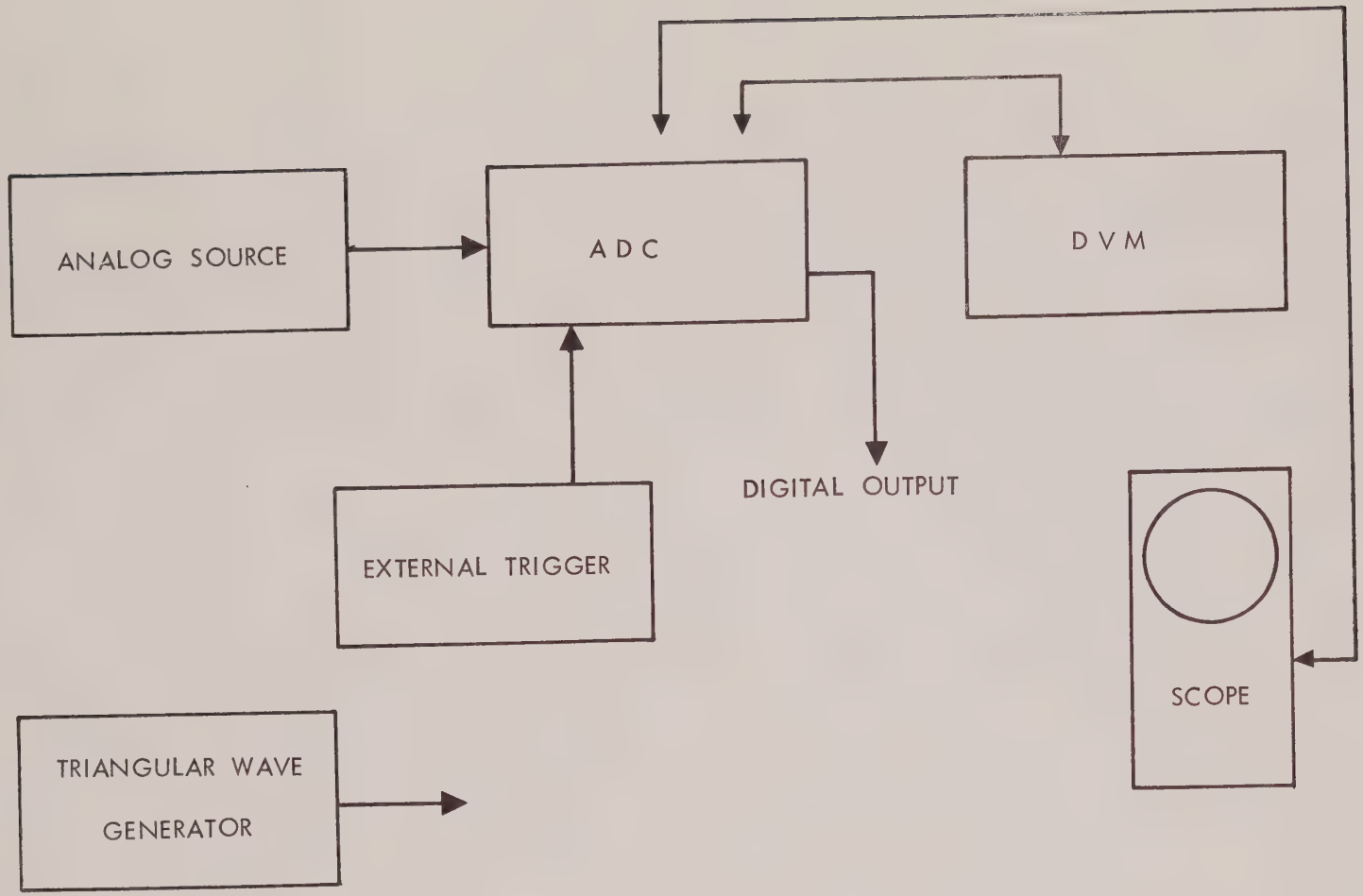


FIGURE 90046

BENCH TEST SETUP

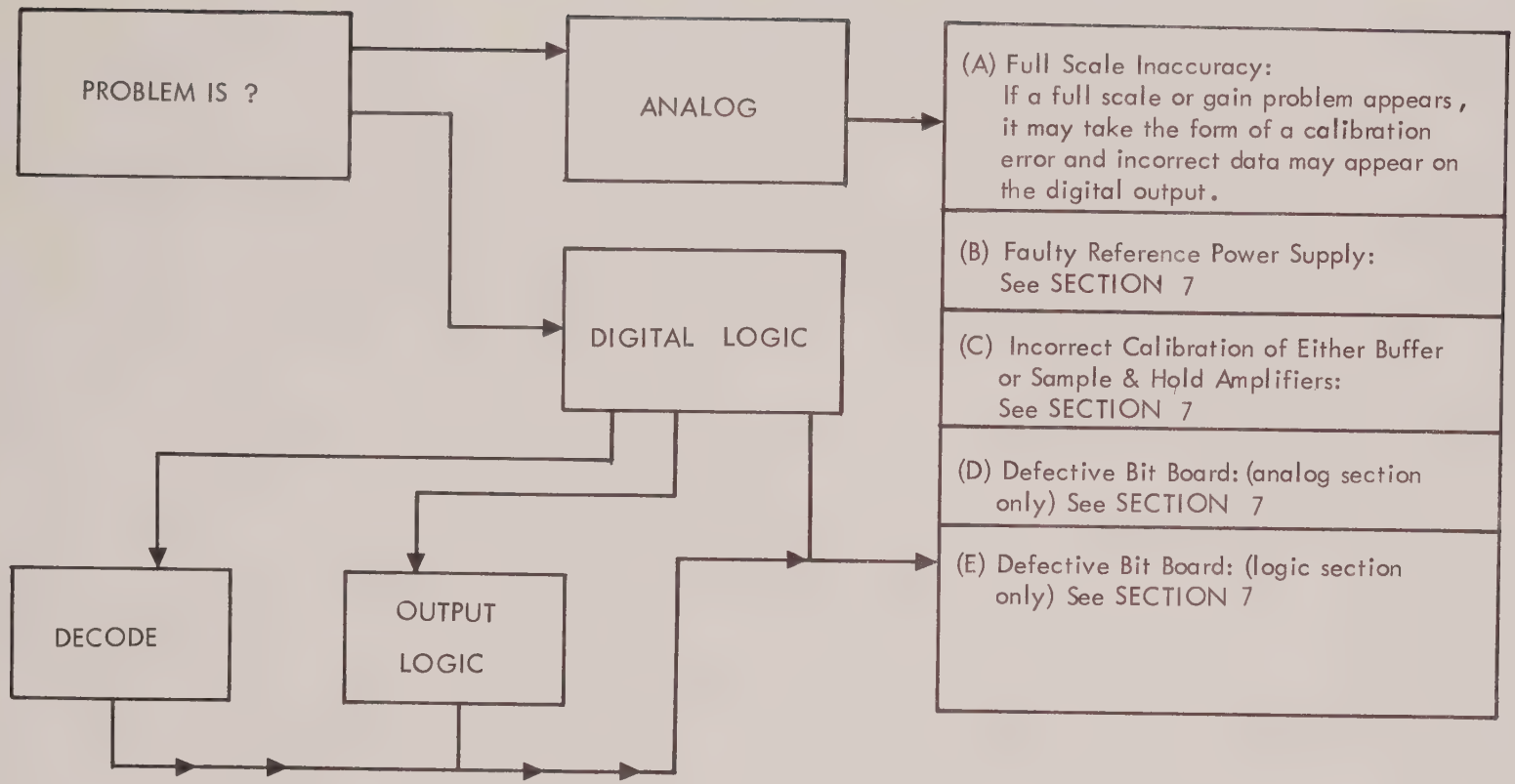


FIGURE 90047

TROUBLESHOOTING FLOW BLOCK DIAGRAM

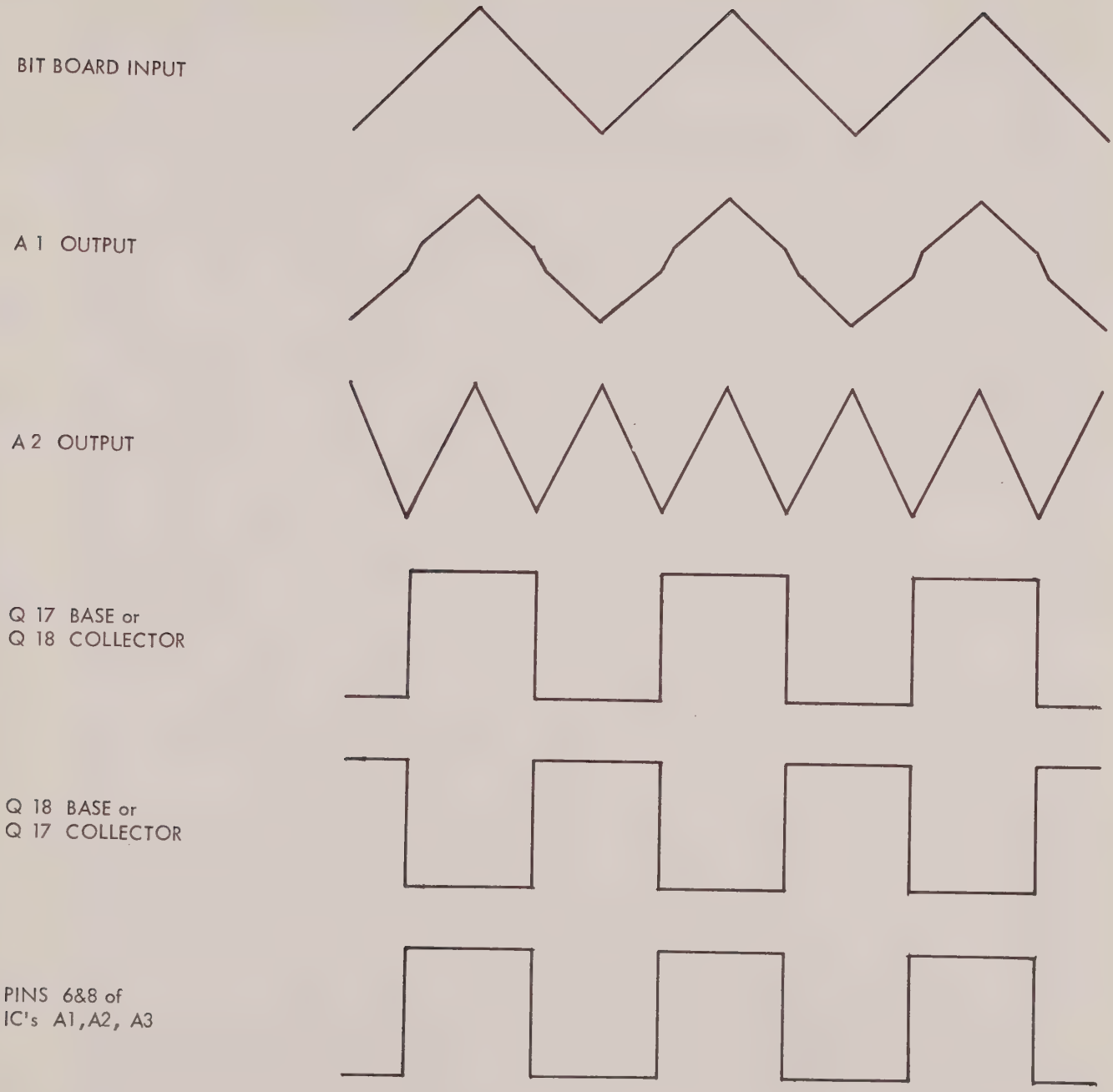


FIGURE 90048

BIT BOARD TYPICAL WAVEFORMS

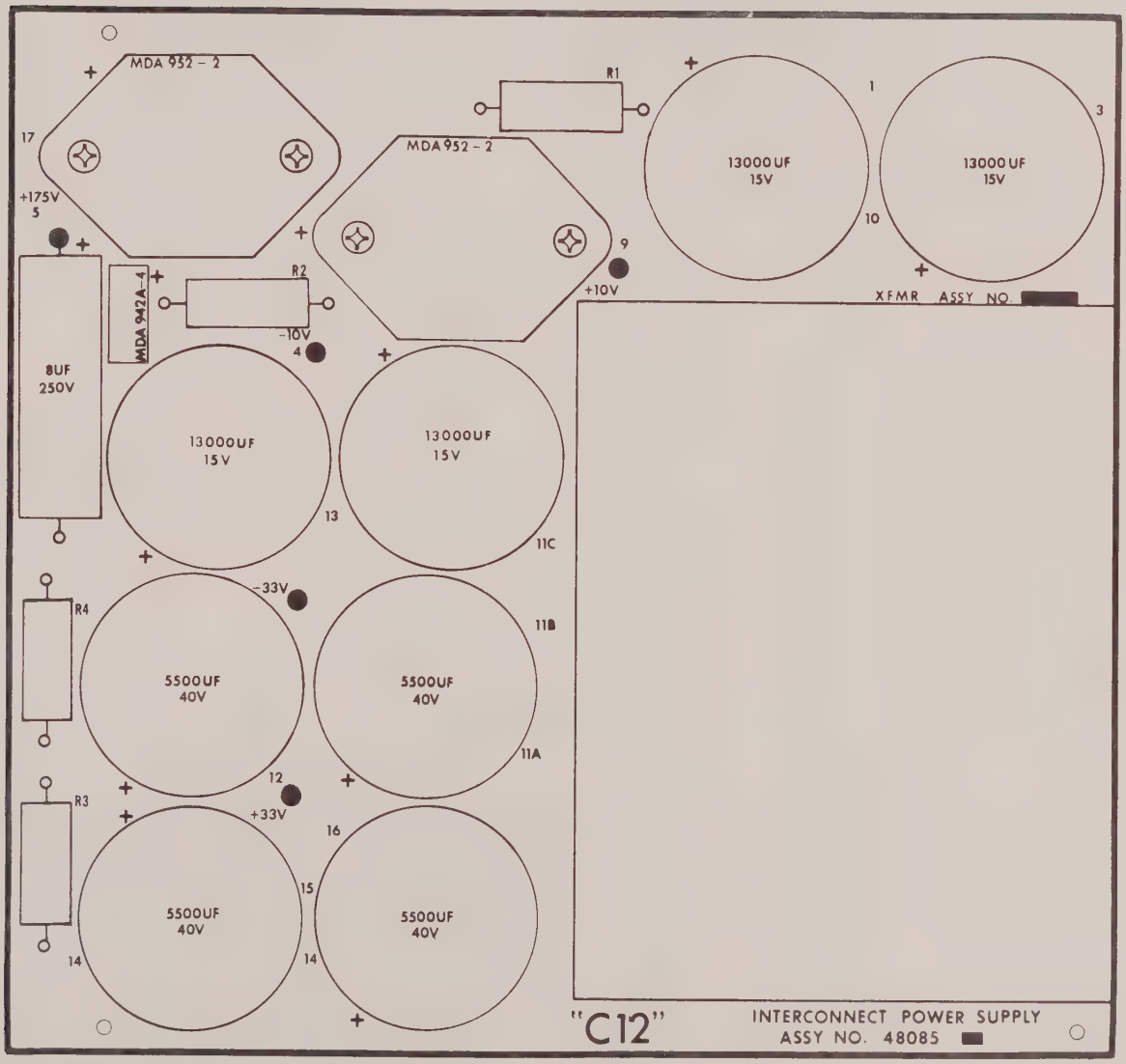
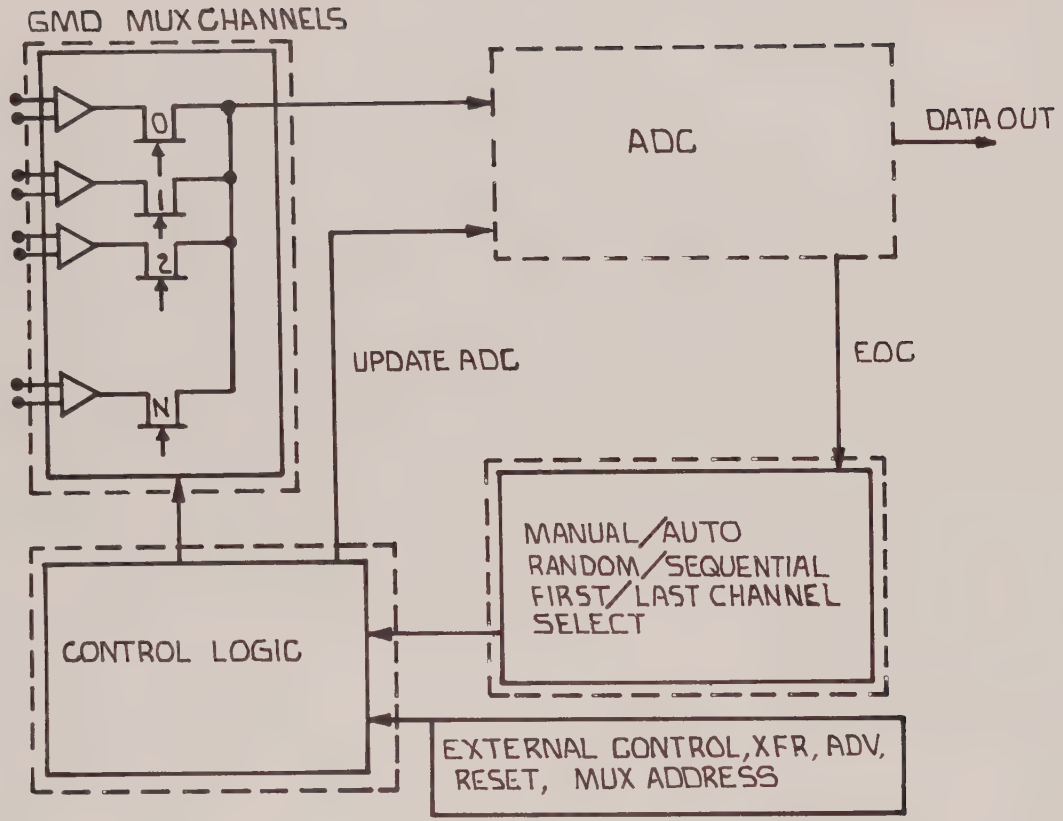


FIGURE 90049

(POWER SUPPLY TEST POINT)



DOTTED LINES INDICATE THE MULTIPLEXER AND ITS CONTROLS MAY BE MOUNTED IN THE SAME MODULE AS THE ADC OR MOUNTED IN A SEPARATE MODULE DEPENDING UPON CUSTOMER REQUIREMENTS

FIGURE 90080
MULTIPLEXER MODULE
BLOCK DIAGRAM

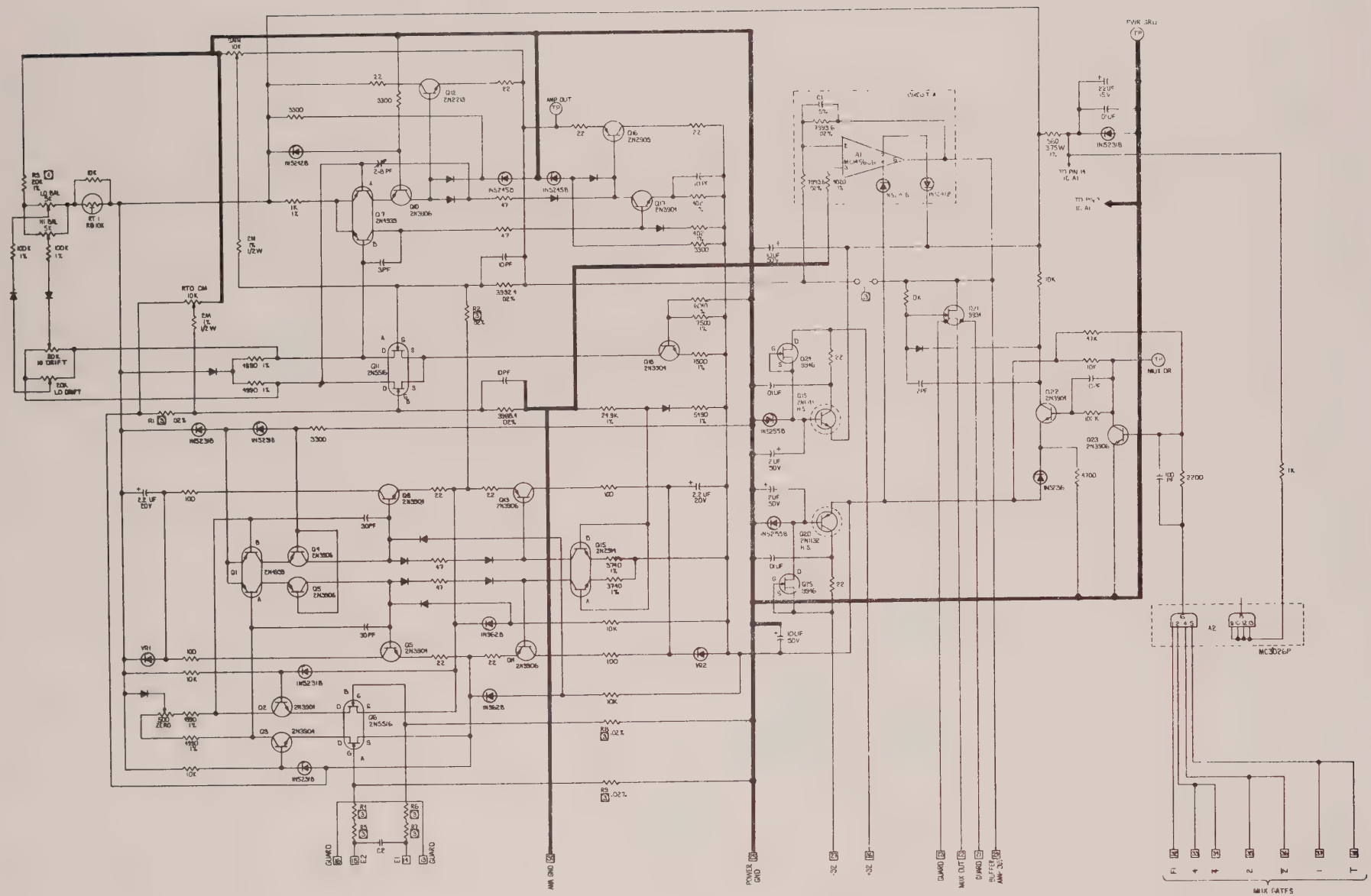


FIGURE 90081

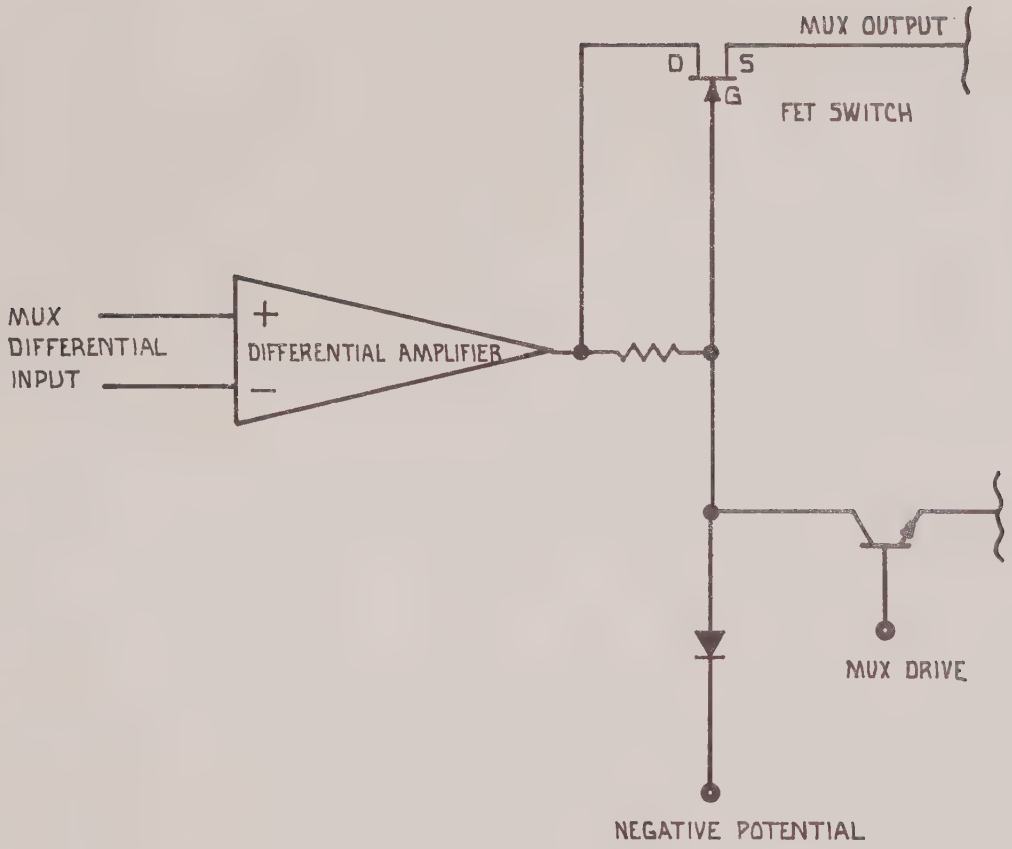


FIGURE 90082

MULTIPLEXER SWITCH BLOCK DIAGRAM

****

FIGURE 90083

THIS FIGURE IS NORMALLY A GENERAL PURPOSE
SCHEMATIC OF A COMMON VERSION OF THE
MODEL GMD-10/1000 AMPLIFIER/MULTIPLEXER.

BECAUSE SMALL CHANGES MAY TAKE PLACE IN THE
SCHEMATIC OF THE AMPLIFIER, WE REFER YOU
TO THE DRAWING IN SECTION (11) OF THIS MANUAL
WHICH CONTAINS THE SCHEMATIC DRAWING
THAT DESCRIBES THE PARTICULAR AMPLIFIER IN
YOUR SYSTEM.

****

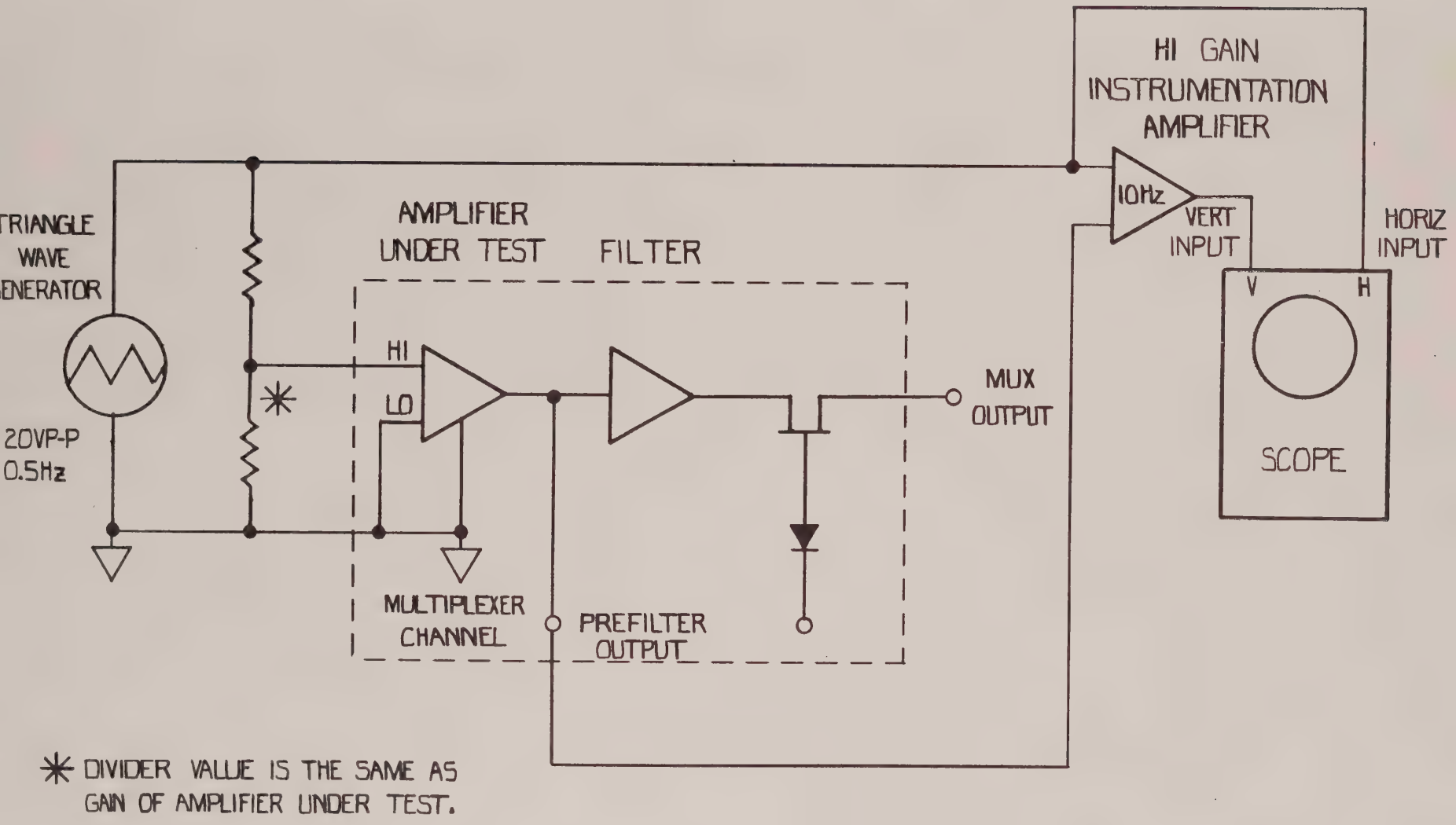


FIGURE 90084

GAIN ADJUSTMENT SET-UP

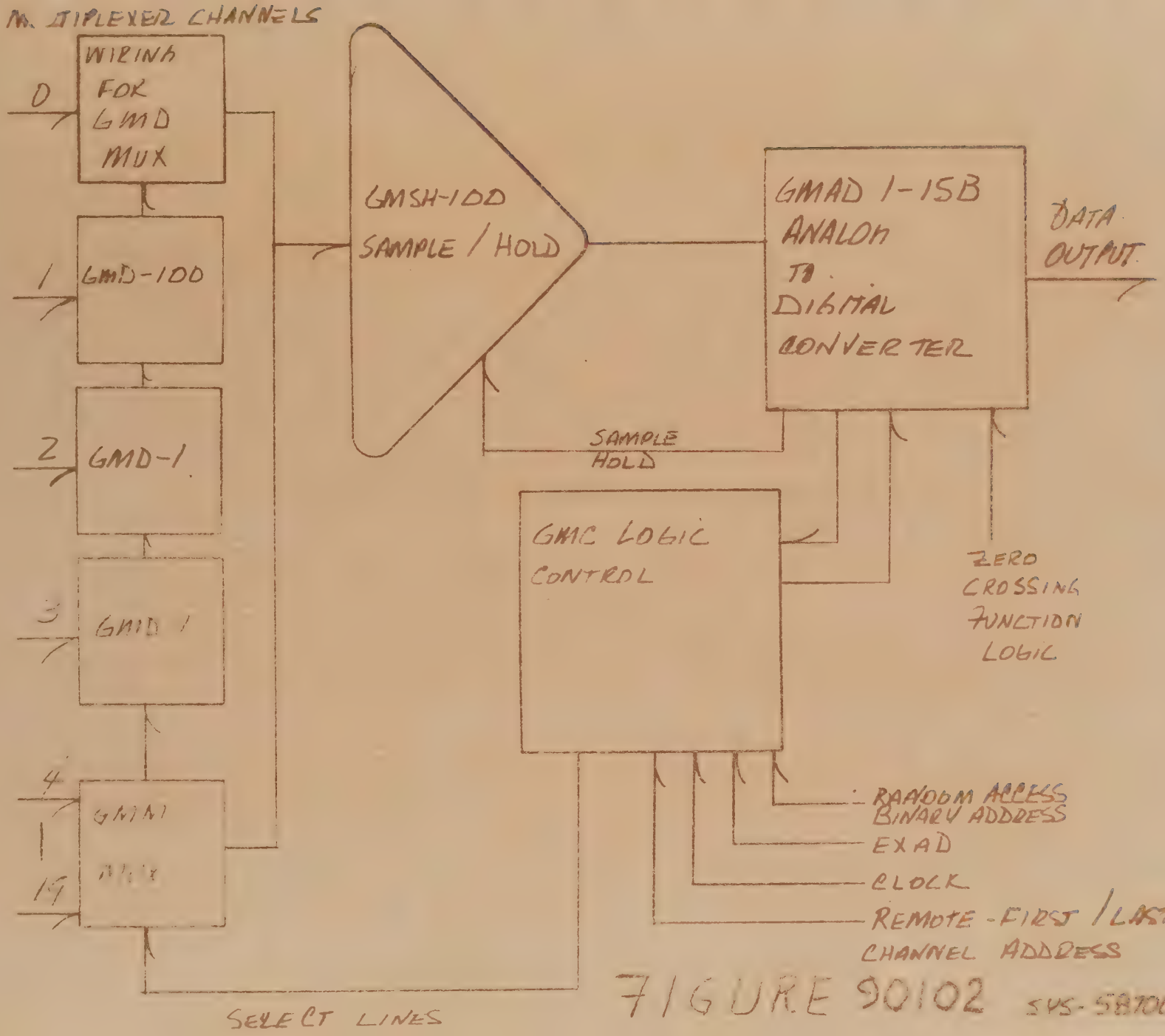
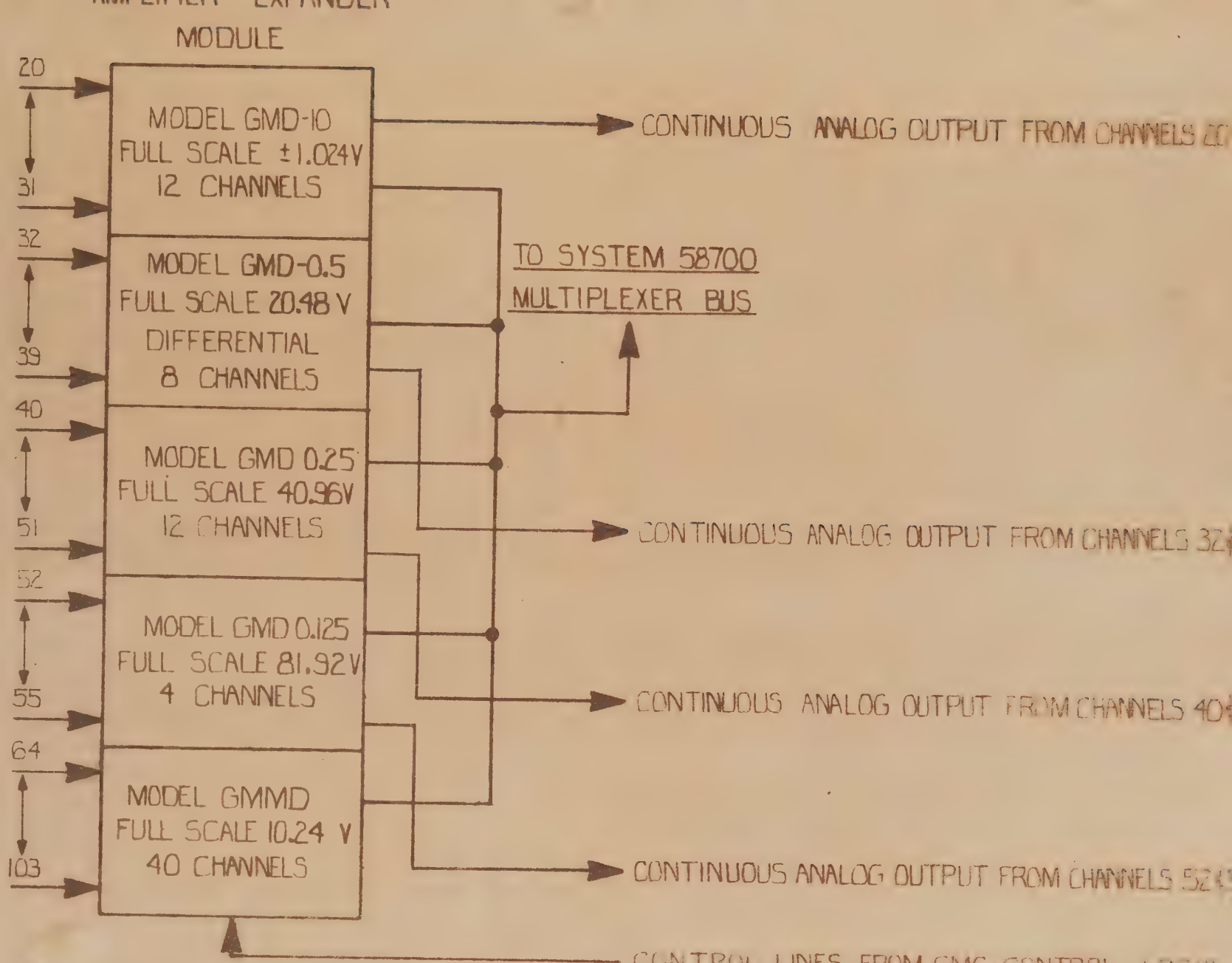


FIGURE 90102 SYS-58100-4015



* 56-63 NOT USED

FIGURE 90103

SYS-58700-58845-4106

BIT BOARD ADJUSTMENTS Figure 7010J

BIT BOARD	ADJUST	INPUT	OUTPUT DATA
5	BO (Z1)	+0.000	10 000 / 01 111
5	Z (Z2)	-0.625	10 000 / 10 001
5	S1 (K2)	-9.375	11 110 / 11 111
5	S2 (K1)	+9.375	00 000 / 00 001
6	BO (Z1)	+0.000	100 000 / 011 111
6	Z (Z2)	-0.313	100 000 / 100 001
6	S1 (K2)	-9.687	111 110 / 111 111
6	S2 (K1)	+9.687	000 000 / 000 001
7	BO (Z1)	+0.000	1 000 000 / 0 111 111
7	Z (Z2)	-0.156	1 000 000 / 1 000 001
7	S1 (K2)	-9.844	1 111 110 / 1 111 111
7	S2 (K1)	+9.844	0 000 000 / 0 000 001
8	Z (Z2)	-0.312	10 000 _____ *
8	BO (Z1)	+0.312	01 111 _____ *
8	S2 (K1)	+9.688	00 000 _____ *
8	S1 (K2)	-9.688	11 111 _____ *
9	Z (Z2)	-0.156	100 000 _____ *
9	BO (Z1)	+0.156	011 111 _____ *
9	S2 (K1)	+9.844	000 000 _____ *
9	S1 (K2)	-9.844	111 111 _____ *
10	Z (Z2)	-0.078	1 000 000 _____ *
10	BO (Z1)	+0.078	0 111 111 _____ *
10	S2 (K1)	+9.922	0 000 000 _____ *
10	S1 (K2)	-9.922	1 111 111 _____ *

11	Z (Z2)	-0.195	10 000 010 ___ *
11	BO (Z1)	+0.117	01 111 110 ___ *
11	S2 (K1)	+9.805	00 000 010 ___ *
11	S1 (K2)	-9.883	11 111 110 ___ *
12	Z (Z2)	-0.0976	100 000 010 ___ *
12	BO (Z1)	+0.0586	011 111 110 ___ *
12	S2 (K1)	+9.9023	000 000 010 ___ *
12	S1 (K2)	-9.9415	111 111 110 ___ *
13	Z (Z2)	-0.0488	1 000 000 010 ___ *
13	BO (Z1)	+0.0293	0 111 111 110 ___ *
13	S2 (K1)	+9.9512	0 000 000 010 ___ *
13	S1 (K2)	-9.9707	1 111 111 110 ___ *
14	Z (Z2)	-0.0244	10 000 000 010 ___ *
14	BO (Z1)	+0.0147	01 111 111 110 ___ *
14	S2 (K1)	+9.9756	00 000 000 010 ___ *
14	S1 (K2)	-9.9854	11 111 111 110 ___ *
15	Z (Z2)	-0.0122	100 000 000 010 ___ *
15	BO (Z1)	+0.0078	011 111 111 110 ___ *
15	S2 (K1)	+9.9881	000 000 000 010 ___ *
15	S1 (K2)	-9.9924	111 111 111 110 ___ *

The 3 least significant bits (___) are used for the transition point recognition. The transition point is the point where the 3 to 4 binary change takes place. The lights will appear to be only partially ON and this should not be confused with the binary number 7 where all indicators are ON full.

WHEN CALIBRATION OF FINAL BOARD IS COMPLETE, A ZERO VOLTS INPUT SHOULD PRODUCE AN ALTERNATION BETWEEN ALL ZERO'S AND ALL ONE'S IN THE READOUT.

IF NOT, REVERSE SIGNS ON ALL CALIBRATION VOLTAGES AND RECALIBRATE THE LAST BOARD ONLY.

THIS CALIBRATION LEAVES 1/2 COUNT OF OFFSET IN THE ADC. THIS OFFSET SHOULD BE REMOVED WITH THE S&H OR BUFFER.

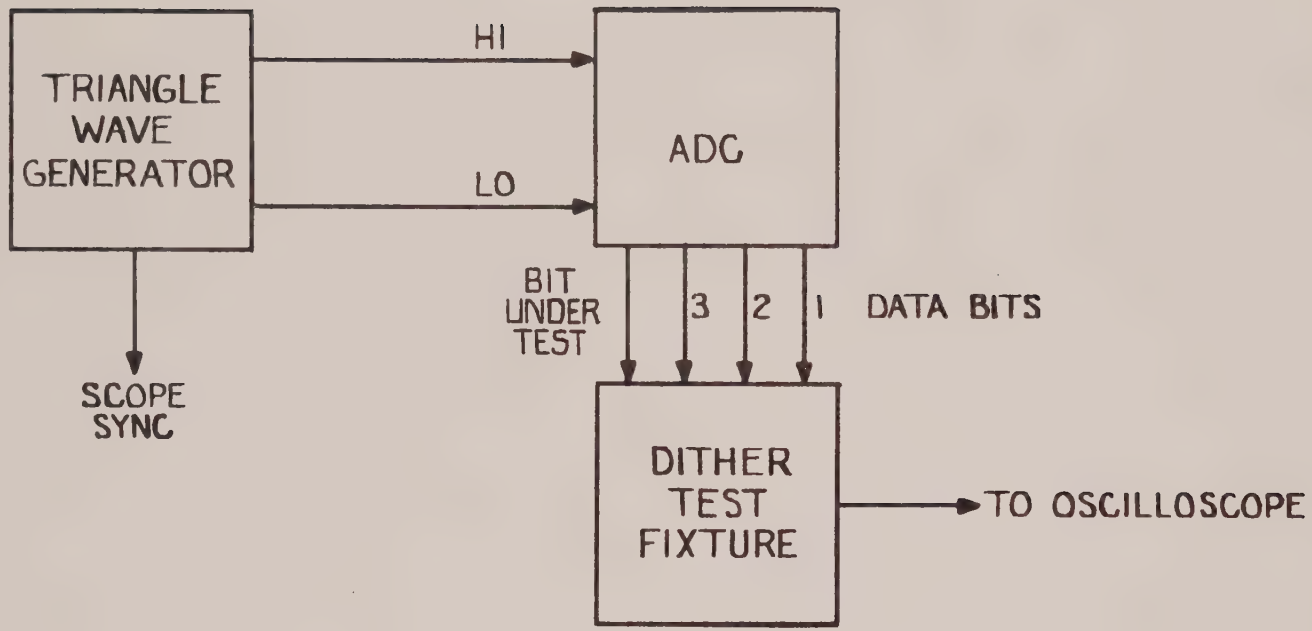


FIGURE 90114
DITHER TEST SET-UP

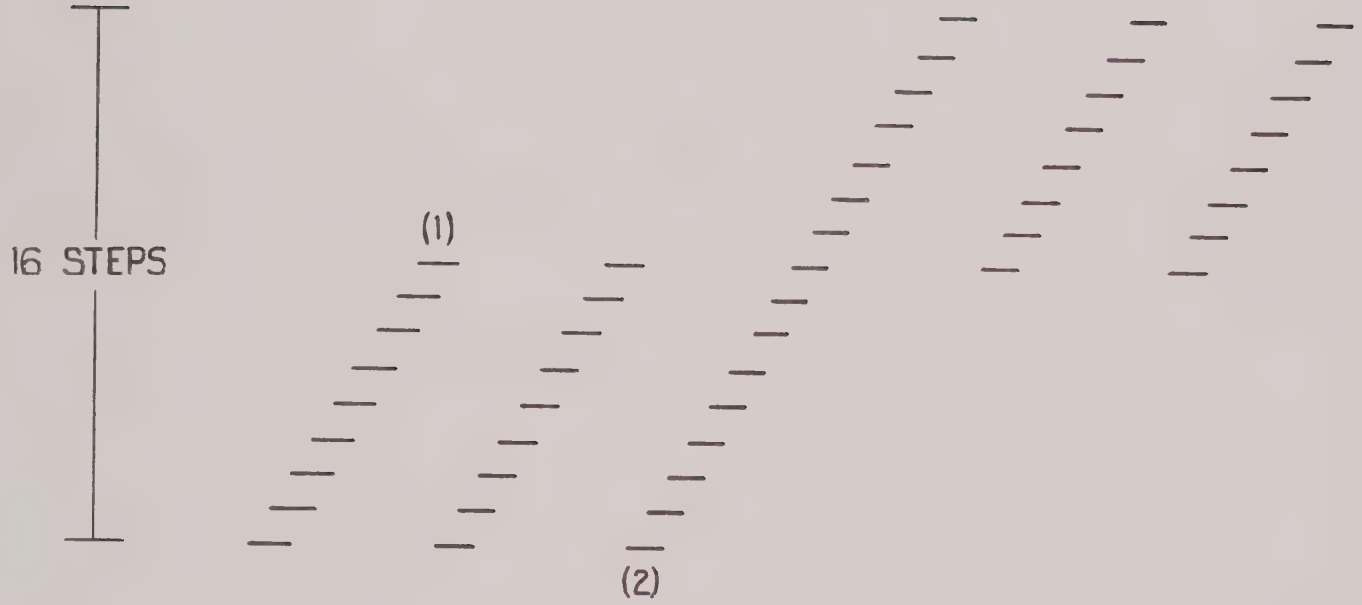
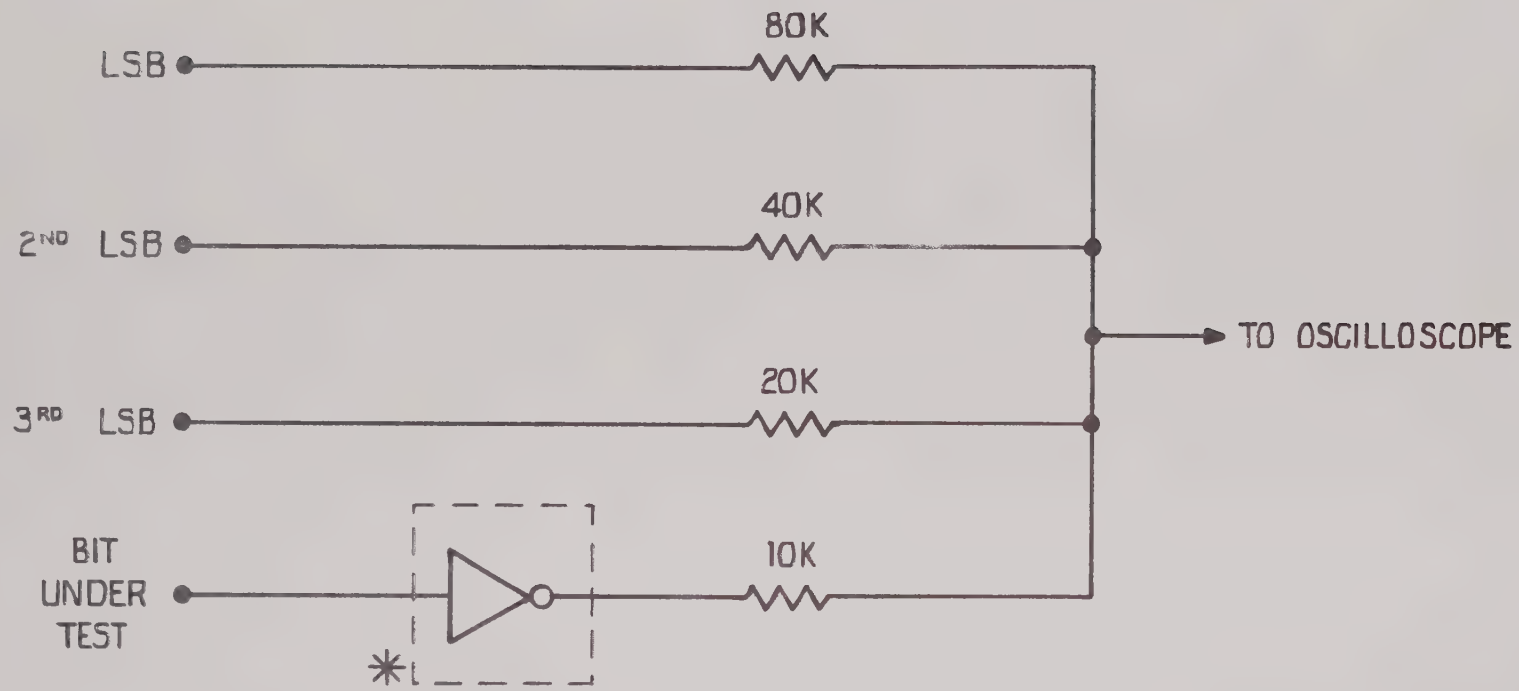


FIGURE 90119

DITHER DISPLAY



* NECESSARY ONLY IF SIGN BIT IS BIT UNDER TEST AND COMPLEMENT OF SIGN BIT IS NOT AVAILABLE AT REAR CONNECTOR

FIGURE 90120

DAC TEST FIXTURE

SECTION 9

TABLES

FRONT PANEL INDICATORS

(14 Bit & Sign) Two's Complement

ADC

FIGURE 90050

Sign	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1		THEORETICAL ANALOG INPUT (% f/s)		CORRESPONDING DC VOLTAGE (Volts) +10v f/s	
-	0	0	0	0	0	0	0	0	0	1	0				*	-f/s	+19.5 cts	-9.9881	1
-	0	0	0	1	1	1	1	1	1	1	0				*	-7/8	-12.5 "	-8.7576	
-	0	0	1	0	0	0	0	0	0	1	0				*	-7/8	+19.5 "	-8.7381	
-	0	0	1	1	1	1	1	1	1	1	0				*	-3/4	-12.5 "	-7.5076	2
-	0	1	0	0	0	0	0	0	0	1	0				*	-3/4	+19.5 "	-7.4881	3
-	0	1	0	1	1	1	1	1	1	1	0				*	-5/8	-12.5 "	-6.2576	
-	0	1	1	0	0	0	0	0	0	1	0				*	-5/8	+19.5 "	-6.2381	
-	0	1	1	1	1	1	1	1	1	1	0				*	-1/2	-12.5 "	-5.0076	4
-	1	0	0	0	0	0	0	0	0	1	0				*	-1/2	+19.5 "	-4.9881	5
-	1	-	-	1	1	1	1	1	1	1	0				*	-3/8	-12.5 "	-3.7576	
-	1	0	1	0	0	0	0	0	0	1	0				*	-3/8	+19.5 "	-3.7381	
-	1	0	1	1	1	1	1	1	1	1	0				*	-1/4	-12.5 "	-2.5076	6
-	1	1	0	0	0	0	0	0	0	1	0				*	-1/4	+19.5 "	-2.4881	7
-	1	1	0	1	1	1	1	1	1	1	0				*	-1/8	-12.5 "	-1.2576	
-	1	1	1	0	0	0	0	0	0	1	0				*	-1/8	+19.5 "	-1.2381	
-	1	1	1	1	1	1	1	1	1	1	0				*	0	-12.5 "	- .0076	8
+	1	0	0	0	0	0	0	0	0	1	0				*	0	+19.5 "	+ .0119	9
+	0	0	0	1	1	1	1	1	1	1	0				*	+1/8	-12.5 "	+1.2424	
+	0	0	1	0	0	0	0	0	0	1	0				*	+1/8	-19.5 "	+1.2519	
+	0	0	1	1	1	1	1	1	1	1	0				*	+1/4	-12.5 "	+2.4924	10
+	0	1	0	0	0	0	0	0	0	1	0				*	+1/4	+19.5 "	+2.5119	11
+	0	1	0	1	1	1	1	1	1	1	0				*	+3/8	-12.5 "	+3.7424	
+	0	1	1	0	0	0	0	0	0	1	0				*	+3/8	+19.5 "	+3.7519	
+	0	1	1	1	1	1	1	1	1	1	0				*	+1/2	-12.5 "	+4.9924	12
+	1	0	0	0	0	0	0	0	0	1	0				*	+1/2	+19.5 "	+5.0119	13
+	1	0	0	1	1	1	1	1	1	1	0				*	+5/8	-12.5 "	+6.2424	
+	1	0	1	0	0	0	0	0	0	1	0				*	+5/8	+19.5 "	+6.2519	
+	1	0	1	1	1	1	1	1	1	1	0				*	+3/4	-12.5 "	+7.4924	14
+	1	1	0	0	0	0	0	0	0	1	0				*	+3/4	-19.5 "	+7.5119	15
+	1	1	0	1	1	1	1	1	1	1	0				*	+7/8	-12.5 "	+8.7424	
+	1	1	1	0	0	0	0	0	0	1	0				*	+7/8	+19.5 "	+8.7519	
+	1	1	1	1	1	1	1	1	1	1	0				*	+f/s	-12.5 cts	+9.9924	16

1 Count = $\frac{f/s}{2N}$ for 10v, 14 bits = $\frac{10}{2^{14}}$ = $\frac{10}{16,384}$ .61mv

12.5 cts = 76 mv

19.5 cts = 119 mv

= $\frac{f/s}{2^N}$

*The 3 least significant bits are used for the transition point recognition. The transition point is the point where the 3 to 4 binary change takes place. The lights will appear to be only partially ON and this should not be confused with the binary number 7 where all 3 indicators are ON full.

TABLE 90051

THE CURVE OF Figure 90029(A) WAS PLOTTED AS FOLLOWS:

POINT	ACTUAL READING	THEORETICAL INPUT	ERROR (mV)	PLOT AT	
1	-9.9877	-9.9881	+0.4	-10	-f/s
2	-7.5080	-7.5076	-0.4	-7.5	-3/4
3	-7.4877	-7.4881	+0.4	-7.5	-3/4
4	-5.0080	-5.0076	-0.4	-5	-1/2
5	-4.9877	-4.9881	+0.4	-5	-1/2
6	-2.5080	-2.5076	-0.4	-2.5	-1/4
7	-2.4877	-2.4881	+0.4	-2.5	-1/4
8	-0.0080	-0.0076	-0.4	0	0
9	+0.0123	+0.0119	+0.4	0	0
10	+2.4920	+2.4924	-0.4	+2.5	+1/4
11	+2.5123	+2.5119	+0.4	+2.5	+1/4
12	+4.9920	+4.9924	-0.4	+5	+1/2
13	+5.0123	+5.0119	+0.4	+5	+1/2
14	+7.4920	+7.4924	-0.4	+7.5	+3/4
15	+7.5123	+7/5119	+0.4	+7.5	+3/4
16	+9.9920	+9.9924	-0.4	+10	+f/s

****

NUMBERS IN EXAMPLE ARE FOR +/- 10V INPUTS. WITH OTHER FULL SCALE VALUES THE NUMBER WILL BE DIFFERENT BUT PROPORTIONAL.

****

SECTION 10

REPLACEMENT PARTS LIST

NOTE:

DUE TO CURRENT DIFFICULTIES IN OBTAINING MANY ELECTRONIC COMPONENTS WITHIN REASONABLE DELIVERY SCHEDULES, SOME COMPONENT VALUES USED IN OUR EQUIPMENT MAY DEVIATE SLIGHTLY FROM THE DOCUMENTED VALUE. IN ALL CASES, IT HAS BEEN PREVIOUSLY VERIFIED THAT SUCH COMPONENT SUBSTITUTIONS WILL NOT DEGRADE THE PERFORMANCE OF THE CIRCUIT OR THE FINAL ASSEMBLY IN ANY MANNER. IN THE EVENT THAT ONE OF THESE SUBSTITUTED COMPONENTS SHOULD REQUIRE REPLACEMENT, THE CUSTOMER MAY USE AS A REPLACEMENT EITHER THE DOCUMENTED COMPONENT OR THE INSTALLED COMPONENT.

PART NO.	QTY	PRICE	DESCRIPTION
8-02	5	1.04	JACK TIP RED
			JOHNSON E F 105-0602-001
8-03	1	1.24	JACK TIP BLACK
			JOHNSON E F 105-0603-001
8-07	1	1.64	CHOKE 1/2W 10% 5.6UH
			MILLER J W 9330-18
17-00	4	2.04	CLAMP CABLE
			AMPHENOL AN 3057-6A
43-05	24	.05	PUSHNUT
			PALNUT PR312075
43-06	2	.02	PUSHNUT
			PALNUT PS250385
47-01	4	.44	CAPACITOR 1PF
			ELMENCO DM15-C-010-D
47-02	141	.44	CAPACITOR 2PF
			ELMENCO DM15-020-D
48-00	119	.44	CAPACITOR 3PF
			ELMENCO DM15-030-D
50-00	1	.44	CAPACITOR 5PF
			ELMENCO DM15-050-D
50-01	36	.40	CAPACITOR 5PF
			ERIE 831-000-C0G0-509C
52-00	2	.40	CAPACITOR 5% 10PF
			ELMENCO DM15-100J
52-01	91	.40	CAPACITOR 5% 10PF
			ERIE 831-000-C0G0-42100D
53-02	2	.40	CAPACITOR 5% 15PF
			ERIE 801-000-C0G0-150J
55-00	26	.45	CAPACITOR 5% 22PF
			ELEMENCO DM15-220J
55-01	47	.40	CAPACITOR 5% 22PF
			ERIE 801-000-C0G0-220J
56-01	30	.44	CAPACITOR 5% 30PF
			ELMENCO DM15-300J
58-01	5	.40	CAPACITOR 10% 47PF
			ERIE 831-000-X5F0-470K
60-01	1	.60	CAPACITOR 10% 68PF
			ERIE 831-000-X5F0-680K
61-01	215	.40	CAPACITOR 10% 100PF
			ERIE 831-000-X5F0-101K
62-00	26	.45	CAPACITOR 5% 100PF
			ELMENCO DM15-101J
63-02	1	.40	CAPACITOR 10% 150PF
			ERIE 831-000-X5F0-151K
64-01	1	.56	CAPACITOR 5% 200PF
			MALLORY SX320
67-01	1	.23	CAPACITOR 10% 220PF
			ERIE 831-000-X5F0-221K
68-03	1	.80	CAPACITOR 10% 330PF
			ERIE 831-000-X5F0-331K

PART NO.	QTY	PRICE	DESCRIPTION
72-01	28	.40	CAPACITOR 10% 470PF ERIE 831-000-X5F0-471K
76-00	4	.96	CAPACITOR 5% 1000PF ELMENCO DM15-102J
76-02	3	.35	CAPACITOR 20% 1000PF ERIE CK60AW102M
77-01	18	2.34	CAPACITOR TRIMMER 9-35PF ERIE 538-006-D9-35
78-01	41	2.34	CAPACITOR TRIMMER 3-15PF ERIE 538-006-D3-15
79-01	15	1.65	CAPACITOR TRIMMER 2-8PF ERIE 538-006A2-8
93-00	1	.48	CAPACITOR 10% .01UF ELMENCO 1DP-1-103
93-01	338	.14	CAPACITOR 10% .01UF ERIE 805-000-X5V0-103Z
111-00	18	.87	CAPACITOR 20% .1UF SPRAGUE 5C023104X0500B3
116-00	114	.72	CAPACITOR 2UF 50V CDE NLW-2-50
120-00	4	2.83	CAPACITOR 20% .47UF ELPAC B1A474
130-01	1	4.85	CAPACITOR 20% 2UF ELPAC B1A205
131-00	252	.84	CAPACITOR 20% 2.2UF 20V SPRAGUE CS13BE225M
133-00	124	1.04	CAPACITOR 20% 2.2UF 35V SPRAGUE CS13BF225M
134-06	26	1.10	CAPACITOR 20% 4.7UF 50V SPRAGUE CS13BG475M
142-00	2	.72	CAPACITOR 10UF 25V CDE NLW-10-25
142-01	32	.85	CAPACITOR 10UF 50V CDE NLW-10-50
144-00	19	.96	CAPACITOR 20% 22UF 15V SPRAGUE CS13BD226M
145-02	8	1.17	CAPACITOR 50UF 50V CDE NLW-50-50
147-00	10	1.50	CAPACITOR 100UF 16V CDE NLW-100-16
147-01	2	.70	CAPACITOR 20% 100UF 20V SPRAGUE CS13BE107M
157-17	8	4.48	CAPACITOR 13000UF 15V SPRAGUE 36D133G015AC2A
157-23	8	5.15	CAPACITOR 5500UF 40V SPRAGUE 36D552G040AC2A
160-05	1	17.78	CONNECTOR 18 PIN HOODED WINCHESTER MRAC-18P-JTC6-H9
161-01	1	8.88	CONNECTOR 18 SOCKET WINCHESTER MRAC-18S-J6

PART NO.	QTY	PRICE	DESCRIPTION
163-04	1	13.73	CONNECTOR 34 PIN HOODED
			WINCHESTER MRAC-34P-JTD-H9
165-00	1	5.93	CONNECTOR 34 SOCKET
			WINCHESTER MRAC-34S-J6
166-02	1	24.55	CONNECTOR 50 PIN HOODED
			WINCHESTER MRAC-50P-JTD-H9
166-04	3	24.55	CONNECTOR 50 PIN HOODED
			WINCHESTER MRAC-50P-JTD-H8
167-00	3	5.95	CONNECTOR 50 SOCKET
			WINCHESTER MRAC-50S-J6
169-00	2	10.75	CONNECTOR 75 SOCKET
			WINCHESTER MRAC-75S-J6
171-03	2	14.88	CONNECTOR 75 PIN HOODED
			WINCHESTER MRAC-75P-JTD-H8
172-02	2	8.95	CONNECTOR 104 SOCKET
			WINCHESTER MRAC-104S-J6
172-03	2	23.55	CONNECTOR 104 PIN HOODED
			WINCHESTER MRAC-104P-JTD-H9
177-00	1	3.40	CONNECTOR 5 PIN
			CANNON MS3102A-14S-5P
178-00	3	3.50	CONNECTOR 5 SOCKET
			CANNON MS3102A-14S-5S
182-02	2	5.60	CONNECTOR FLANGED INLET
			ARROW-HART 7486
191-00	2	7.90	CONNECTOR 5 SOCKET
			CANNON MS3107A-14S-5S
192-00	3	9.10	CONNECTOR 5 PIN
			CANNON MS3107A-14S-5P
232-03	2	.56	DIODE ZENER 1N5227B
			MOTOROLA 1N5227B
234-02	7	.43	DIODE ZENER 1N5235B
			MOTOROLA 1N5235B
235-01	5	.48	DIODE ZENER 1N5239B
			MOTOROLA 1N5239B
237-00	70	.40	DIODE ZENER 1N5242B
			MOTOROLA 1N5242B
238-00	1	9.95	DIODE ZENER 1N825
			MOTOROLA 1N825
239-00	935	.11	DIODE 1N4148
			1N4148
239-01	193	.20	DIODE 1N914B
			FAIRCHILD 1N914B
240-80	32	.40	DIODE ZENER 1N962B
			MOTOROLA 1N962B
244-01	1	.19	DIODE 1N4001
			MOTOROLA 1N4001
244-03	4	.43	DIODE ZENER 1N5223B
			MOTOROLA 1N5223B
244-04	1	.60	DIODE ZENER 1N5221B
			MOTOROLA 1N5221B

PART NO.	QTY	PRICE	DESCRIPTION	
244-08	52	.40	DIODE ZENER	1N5232B
			MOTOROLA	1N5232B
246-01	4	8.25	RECTIFIER BRIDGE	MDA952-2
			MOTOROLA	MDA952-2
247-20	124	.40	DIODE ZENER	1N5255B
			MOTOROLA	1N5255B
248-06	103	.43	DIODE ZENER	1N5231B
			MOTOROLA	1N5231B
248-07	9	1.04	DIODE ZENER	1N5236B
			MOTOROLA	1N5236B
248-08	11	.43	DIODE ZENER	1N5234B
			MOTOROLA	1N5234B
248-10	38	.40	DIODE ZENER	1N5240B
			MOTOROLA	1N5240B
248-12	34	.40	DIODE ZENER	1N5245B
			MOTOROLA	1N5245B
248-13	14	.04	DIODE ZENER	1N5241B
			MOTOROLA	1N5241B
248-14	29	.43	DIODE ZENER	1N5237B
			MOTOROLA	1N5237B
248-20	20	.43	DIODE ZENER	1N5253B
			MOTOROLA	1N5253B
248-22	20	2.85	DIODE	5082-2810
			HEWLETT PACK	5082-2810
248-26	23	.76	DIODE L.E.D.	135-3510
			ELDEMA	135-3510 (ALT FLV111
248-27	20	2.25	DIODE	5082-2800
			HEWLETT PACK	5082-2800
256-04	2	23.75	FAN	
			IMC	WS2107FL
257-01	4	5.18	FINGER GUARD	
			PAMOTOR	5504
261-02	8	1.41	FERRULE HANDLE	
			USECO	904-17
261-14	100	.45	FERRULE TERMASHIELD	
			AMP	323932
262-00	200	.45	FERRULE	
			AMP	323930
266-01	1	1.32	FUSE 2AMP 3AG SLO-BLO	
			LITTLEFUSE	313002
267-01	1	1.52	FUSE 3AMP 3AG SLO-BLO	
			LITTLEFUSE	313003
274-00	2	1.60	FUSEHOLDER	
			LITTLEFUSE	342004
280-05	4	6.50	HANDLE CABINET	
			USECO	1093-17
284-01	60	.60	HEAT SINK	
			IERC	TXBF-032-025B
296-00	82	.26	NUT LOCK 4-40	
			ANY	NAS679-A04

PART NO.	QTY	PRICE	DESCRIPTION	
297-00	60	.29	NUT LOCK 6-32	
			ANY	NAS679-A06
298-00	4	.03	NUT LOCK 8-32	
			ANY	NAS679-A08
299-00	8	.26	NUT LOCK 10-32	
			ANY	NAS679-A3
313-00	8	.10	NUT 8-32	
			WALLACE	AN340-C8
318-00	107	.06	NUT 4-40	
			WALLACE	NAS-671-C4
318-01	156	.08	NUT 4-40	
			COML	
326-00	37	.25	TRANSISTOR PAD	
			MILTON ROSS	10099-N
327-00	34	.21	TRANSISTOR PAD	
			DELBERT BLIN	606-600-D
331-00	610	.44	CONTACT PIN	
			WINCHESTER	100-2020P
332-00	560	1.06	CONTACT SOCKET	
			WINCHESTER	100-2020S
340-07	2	2.70	POTENTIOMETER	20
			SPECTROL	43P-200
341-04	1	3.38	POTENTIOMETER	100
			SPECTROL	62-2-1-101
342-01	13	2.70	POTENTIOMETER	100
			SPECTROL	43P-101
344-07	5	3.13	POTENTIOMETER	500
			SPECTROL	43P-501
344-80	9	2.76	POTENTIOMETER	500
			SPECTROL	62-2-1-501
346-80	11	3.13	POTENTIOMETER	2K
			SPECTROL	62-2-1-202
347-01	16	2.55	POTENTIOMETER	2K
			SPECTROL	43P-202
351-80	33	2.61	POTENTIOMETER	5K
			SPECTROL	62-2-1-502
352-01	20	2.13	POTENTIOMETER	5K
			SPECTROL	43P-502
358-80	4	2.63	POTENTIOMETER	10K
			SPECTROL	62-2-1-103
359-03	54	2.55	POTENTIOMETER	10K
			SPECTROL	43P-103
360-03	26	2.76	POTENTIOMETER	20K
			SPECTROL	62-2-1-203
361-01	1	2.61	POTENTIOMETER	25K
			SPECTROL	62-2-1-253
361-81	2	2.61	POTENTIOMETER	25K
			SPECTROL	62-3-1-253
362-00	1	1.90	POTENTIOMETER	50K
			PRESTON	12004

PART NO.	QTY	PRICE	DESCRIPTION
369-02	20	2.61	POTENTIOMETER 50K SPECTROL 62-2-1-503
372-03	83	2.25	POTENTIOMETER 50K SPECTROL 43P-503
373-04	4	2.55	POTENTIOMETER 100K SPECTROL 43P-104
374-02	6	2.55	THERMISTOR 5K FENWAL JA-35J1
374-04	1	2.55	THERMISTOR 1K FENWAL JB-31J1
374-05	18	1.62	THERMISTOR 10K FENWAL JA-41J1
386-03	24	.49	RESISTOR 1/8W 1% 402 CORNING NC4-4020-F
387-07	10	.49	RESISTOR 1/8W 1% 2490 CORNING NC4-2491-F
387-08	2	.49	RESISTOR 1/8W 1% 1K CORNING NC4-1001-F
387-09	1	.49	RESISTOR 1/8W 1% 1180 CORNING NC4-1181-F
388-02	22	.49	RESISTOR 1/8W 1% 3740 CORNING NC4-3741-F
389-01	44	.49	RESISTOR 1/8W 1% 4990 CORNING NC4-4991-F
389-02	3	.49	RESISTOR 1/8W 1% 5490 CORNING NC4-5491-F
390-03	11	.49	RESISTOR 1/8W 1% 6040 CORNING NC4-6041-F
390-04	12	.49	RESISTOR 1/8W 1% 7500 CORNING NC4-7501-F
390-05	15	.49	RESISTOR 1/8W 1% 10K CORNING NC4-1002-F
390-15	5	.49	RESISTOR 1/8W 1% 12.1K CORNING NC4-1212-F
390-19	5	.49	RESISTOR 1/8W 1% 14.7K CORNING NC4-1472-F
391-01	52	.49	RESISTOR 1/8W 1% 16.2K CORNING NC4-1622-F
392-00	63	.49	RESISTOR 1/8W 1% 20K CORNING NC4-2002-F
392-01	63	.49	RESISTOR 1/8W 1% 24.9K CORNING NC4-2492-F
393-05	178	.49	RESISTOR 1/8W 1% 100K CORNING NC4-1003-F
394-12	8	.49	RESISTOR 1/4W 1% 49.9 CORNING NC5-49R9-F
394-22	2	.49	RESISTOR 1/4W 1% 61.9 CORNING NC5-61R9-F
395-13	1	.49	RESISTOR 1/4W 1% 88.7 CORNING NC5-88R7-F

PART NO.	QTY	PRICE	DESCRIPTION
397-13	3	.49	RESISTOR 1/4W 1% 100 CORNING NC5-1000-F
401-04	34	.49	RESISTOR 1/4W 1% 402 CORNING NC5-4020-F
401-28	5	.49	RESISTOR 1/4W 1% 280 CORNING NC5-2800-F
402-01	1	.49	RESISTOR 1/4W 1% 523 CORNING NC5-5230-F
402-02	28	.49	RESISTOR 1/4W 1% 499 CORNING NC5-4990-F
405-00	12	.49	RESISTOR 1/4W 1% 590 CORNING NC5-5900-F
405-01	8	.49	RESISTOR 1/4W 1% 619 CORNING NC5-6190-F
407-00	4	.49	RESISTOR 1/4W 1% 750 CORNING NC5-7500-F
408-00	3	.49	RESISTOR 1/4W 1% 806 CORNING NC5-8060-F
408-03	5	.49	RESISTOR 1/4W 1% 887 CORNING NC5-8870-F
409-00	33	.49	RESISTOR 1/4W 1% 1K CORNING NC5-1001-F
413-00	6	.49	RESISTOR 1/4W 1% 1240 CORNING NC5-1241-F
414-00	4	.49	RESISTOR 1/4W 1% 1370 CORNING NC5-1371-F
421-00	1	.49	RESISTOR 1/4W 1% 1870 CORNING NC5-1871-F
422-00	25	.49	RESISTOR 1/4W 1% 2K CORNING NC5-2001-F
425-00	1	.49	RESISTOR 1/4W 1% 2370 CORNING NC5-2371-F
427-00	15	.49	RESISTOR 1/4W 1% 2490 CORNING NC5-2491-F
436-02	1	.49	RESISTOR 1/4W 1% 3320 CORNING NC5-3321-F
439-01	10	.48	RESISTOR 1/4W 1% 3740 CORNING NC5-3741-F
439-02	1	.49	RESISTOR 1/4W 1% 3920 CORNING NC5-3921-F
440-00	29	.49	RESISTOR 1/4W 1% 4020 CORNING NC5-4021-F
444-00	1	.44	RESISTOR 1/4W 1% 4870 CORNING NC5-4871-F
445-00	33	.49	RESISTOR 1/4W 1% 4990 CORNING NC5-4991-F
445-02	2	.44	RESISTOR 1/4W 1% 5360 CORNING NC5-5361-F
446-00	3	.49	RESISTOR 1/4W 1% 5490 CORNING NC5-5491-F

PART NO.	QTY	PRICE	DESCRIPTION
446-10	2	.49	RESISTOR 1/4W 1% 5620 CORNING NC5-5621-F
448-00	101	.49	RESISTOR 1/4W 1% 6040 CORNING NC5-6041-F
451-06	20	.49	RESISTOR 1/4W 1% 7500 CORNING NC5-7501-F
455-01	5	.49	RESISTOR 1/4W 1% 9530 CORNING NC5-9531-F
456-01	1	.49	RESISTOR 1/4W 1% 10.2K CORNING NC5-1022-F
456-03	17	.49	RESISTOR 1/4W 1% 10K CORNING NC5-1002-F
458-01	5	.49	RESISTOR 1/4W 1% 11.5K CORNING NC5-1152-F
459-00	6	.49	RESISTOR 1/4W 1% 12.4K CORNING NC5-1242-F
460-03	96	.49	RESISTOR 1/4W 1% 15.8K CORNING NC5-1582-F
463-00	96	.49	RESISTOR 1/4W 1% 18.2K CORNING NC5-1822-F
465-02	14	.49	RESISTOR 1/4W 1% 20K CORNING NC5-2002-F
465-05	1	.49	RESISTOR 1/4W 1% 20.5K CORNING NC5-2052-F
467-01	1	.49	RESISTOR 1/4W 1% 28.7K CORNING NC5-2872-F
467-03	6	.49	RESISTOR 1/4W 1% 24.9K CORNING NC5-2492-F
468-01	3	.48	RESISTOR 1/4W 1% 29.4K CORNING NC5-2942-F
469-00	2	.49	RESISTOR 1/4W 1% 33.2K CORNING NC5-3322-F
469-01	1	.49	RESISTOR 1/4W 1% 34K CORNING NC5-3402-F
471-03	9	.49	RESISTOR 1/4W 1% 40.2K CORNING NC5-4022-F
472-25	2	.49	RESISTOR 1/4W 1% 49.9K CORNING NC5-4992-F
475-02	1	.45	RESISTOR 1/4W 1% 78.7K CORNING NC5-7872-F
476-00	2	.44	RESISTOR 1/4W 1% 82.5K CORNING NC5-8252-F
477-25	5	.49	RESISTOR 1/4W 1% 124K CORNING NC5-1243-F
478-00	10	.49	RESISTOR 1/4W 1% 100K CORNING NC5-1003-F
478-05	3	.49	RESISTOR 1/4W 1% 154K CORNING NC5-1543-F
478-16	6	.49	RESISTOR 1/4W 1% 133K CORNING NC5-1333-F

PART NO.	QTY	PRICE	DESCRIPTION
479-00	9	.49	RESISTOR 1/4W 1% 200K
			CORNING NC5-2003-F
479-02	3	.45	RESISTOR 1/4W 1% 249K
			CORNING NC5-2493-F
481-02	2	.49	RESISTOR 1/4W 1% 332K
			CORNING NC5-3323-F
483-00	2	.49	RESISTOR 1/4W 1% 392K
			CORNING NC5-3923-F
483-03	2	.49	RESISTOR 1/4W 1% 402K
			CORNING NC5-4023-F
484-00	8	.49	RESISTOR 1/4W 1% 499K
			CORNING NC5-4993-F
488-02	2	2.55	RESISTOR 1/4W 1% 2.49M
			DALE DC-1/4
488-11	12	.49	RESISTOR 1/2W 1% 2M
			CORNING NC6-2004-F
488-16	38	.49	RESISTOR 1/4W 1% 1M
			CORNING NC5-1004-F
488-20	10	1.80	RESISTOR 1/8W 1% 2M
			DALE DC-1/8
494-05	3	.49	RESISTOR 1/2W 1% 806
			CORNING NC6-8060-F
495-00	9	.49	RESISTOR 1/2W 1% 1K
			CORNING NC6-1001-F
495-06	3	.49	RESISTOR 1/2W 1% 1580
			CORNING NC6-1581-F
496-02	3	.49	RESISTOR 1/2W 1% 3160
			CORNING NC6-3161-F
496-05	3	.49	RESISTOR 1/2W 1% 3240
			CORNING NC6-3241-F
520-00	105	.11	RESISTOR 1/4W 10% 10
			ALLEN-BRADLE CB1001
521-00	371	.11	RESISTOR 1/4W 10% 22
			ALLEN-BRADLE CB2201
522-00	34	.11	RESISTOR 1/4W 10% 33
			ALLEN-BRADLE CB3301
523-00	145	.17	RESISTOR 1/4W 10% 47
			ALLEN-BRADLE CB4701
525-00	251	.11	RESISTOR 1/4W 10% 100
			ALLEN-BRADLE CB1011
525-03	3	.40	RESISTOR 1/4W 10% 150
			ALLEN-BRADLE CB1511
526-00	23	.11	RESISTOR 1/4W 10% 180
			ALLEN-BRADLE CB1811
527-00	33	.11	RESISTOR 1/4W 10% 220
			ALLEN-BRADLE CB2211
528-00	10	.11	RESISTOR 1/4W 10% 330
			ALLEN-BRADLE CB3311
529-00	105	.11	RESISTOR 1/4W 10% 470
			ALLEN-BRADLE CB4711

PART NO.	QTY	PRICE	DESCRIPTION
530-00	2	.11	RESISTOR 1/4W 10% 680
			ALLEN-BRADLE CB6811
531-00	235	.11	RESISTOR 1/4W 10% 1K
			ALLEN-BRADLE CB1021
533-00	76	.11	RESISTOR 1/4W 10% 2200
			ALLEN-BRADLE CB2221
534-00	2	.11	RESISTOR 1/4W 10% 2700
			ALLEN-BRADLE CB2721
535-00	169	.11	RESISTOR 1/4W 10% 3300
			ALLEN-BRADLE CB3321
536-00	127	.11	RESISTOR 1/4W 10% 4700
			ALLEN-BRADLE CB4721
537-00	3	.11	RESISTOR 1/4W 10% 6800
			ALLEN-BRADLE CB6821
538-00	491	.11	RESISTOR 1/4W 10% 10K
			ALLEN-BRADLE CB1031
540-00	64	.11	RESISTOR 1/4W 10% 15K
			ALLEN-BRADLE CB1531
541-00	22	.11	RESISTOR 1/4W 10% 22K
			ALLEN-BRADLE CB2231
544-00	125	.11	RESISTOR 1/4W 10% 47K
			ALLEN-BRADLE CB4731
546-00	2	.11	RESISTOR 1/4W 10% 68K
			ALLEN-BRADLE CB6831
547-00	148	.11	RESISTOR 1/4W 10% 100K
			ALLEN-BRADLE CB1041
551-00	1	.11	RESISTOR 1/4W 10% 1M
			ALLEN-BRADLE CB1051
555-00	28	.11	RESISTOR 1/4W 10% 4.7M
			ALLEN-BRADLE CB4751
555-01	31	.11	RESISTOR 1/4W 10% 10M
			ALLEN-BRADLE CB1061
558-04	4	.22	RESISTOR 1/2W 5% 1
			ALLEN-BRADLE EB10G5
558-06	8	.22	RESISTOR 1/2W 5% 2
			ALLEN-BRADLE EB20G5
558-08	1	.52	RESISTOR 1/2W 5% 3
			ALLEN-BRADLE EB30G5
559-00	3	.11	RESISTOR 1/2W 10% 4.7
			ALLEN-BRADLE EB47G1
560-00	7	.10	RESISTOR 1/2W 10% 10
			ALLEN-BRADLE EB1001
561-00	41	.12	RESISTOR 1/2W 10% 22
			ALLEN-BRADLE EB2201
563-00	10	.11	RESISTOR 1/2W 10% 47
			ALLEN-BRADLE EB4701
565-00	7	.10	RESISTOR 1/2W 10% 100
			ALLEN-BRADLE EB1011
566-00	8	.29	RESISTOR 1/2W 10% 150
			ALLEN-BRADLE EB1511

PART NO.	QTY	PRICE	DESCRIPTION
602-09	4	2.22	RESISTOR3.75W 1% 560
			DALE RS-2B
607-04	96	.32	RESISTOR 2W 10% 100
			ALLEN-BRADLE HB1011
608-00	6	1.56	RESISTOR 3W 5% 1
			SPRAGUE 242E1R05
608-03	1	2.40	RESISTOR 3W 5% .5
			DALE RS-2B
608-07	1	1.95	RESISTOR 3W 5% 2
			SPRAGUE 450E2R05
609-80	48	1.44	RESISTOR 5W 5% 20
			SPRAGUE 243E2005
609-95	1	2.19	RESISTOR 5W 5% .5
			DALE RS-5
624-00	24	.05	SCREW FILL 4-40 X 3/8
			ANY AN500D-4-6
641-00	60	.05	SCREW FHMS 6-32 X 3/8
			ANY AN507C-632-R6
655-02	4	.17	SCREW SET 4-40 X 1/8
			ANY AN565-D4-H2
659-00	44	.03	SCREW PHMS 2-56 X 5/16
			ANY MS35216-4
663-00	2	.45	SCREW PHMS 4-40 X 3/16
			ANY MS35216-11
665-00	135	.04	SCREW PHMS 4-40 X 5/16
			ANY MS35216-13
666-00	93	.04	SCREW PHMS 4-40 X 3/8
			ANY MS35216-14
667-00	6	.05	SCREW PHMS 4-40 X 7/16
			ANY MS35216-15
668-00	156	.05	SCREW PHMS 4-40 X 1/2
			ANY MS35216-16
672-00	8	.07	SCREW PHMS 4-40 X 1
			ANY MS35216-20
675-00	4	.05	SCREW PHMS 6-32 X 3/8
			ANY MS35216-25
679-00	16	.09	SCREW PHMS 6-32 X 3/4
			ANY MS35216-29
700-00	8	.25	SCREW HEX 10-32 X 5/8
			ANY TF538C-1032-10
721-03	2	3.10	SOCKET 8 PIN
			AUGAT 8058-1G49
724-00	40	.24	SCREW HEX HD 10-32 X 3/8
			WALLACE TF538C-1032-6
754-01	2	3.68	SWITCH TOGGLE
			CUTLER/HAM 8360K7
756-02	2	3.30	SWITCH PUSHBUTTON
			C&K P8121-2/DRESS NUT
764-01	14	2.80	SWITCH TOGGLE
			C&K 7101/DRESSNUT

PRICES SUBJECT TO CHANGE WITHOUT NOTICE

PART NO.	QTY	PRICE	DESCRIPTION	
793-00	1	.26	LUG CRIMP	
			AMP	320882
794-00	8	.44	LUG CRIMP	
			AMP	31881
800-02	2	3.73	THERMOSTAT	
			TEXAS INST	20700L79-648L155-2.5
824-00	52	1.24	TRANSISTOR	2N1132
			MOTOROLA	2N1132
828-00	88	1.12	TRANSISTOR	2N1711
			RAYTHEON	2N1711
830-02	36	1.12	TRANSISTOR	2N2219A
			NATIONAL	2N2219A
838-02	21	.90	TRANSISTOR	2N2905A
			NATIONAL	2N2905A
838-04	16	3.13	TRANSISTOR	2N2914
			MOTOROLA	2N2914
839-00	2	3.95	TRANSISTOR	2N2916
			TEXAS INST	2N2916
842-01	10	.80	TRANSISTOR	2N4264
			MOTOROLA	2N4264
845-05	8	9.00	TRANSISTOR SELECTED	9932
			SILICONIX	9932
845-08	2	4.00	TRANSISTOR	DN1011
			SILICONIX	DN1011
845-10	15	6.60	TRANSISTOR	E7001
			SILICONIX	E7001
846-00	524	.37	TRANSISTOR	2N3904
			MOTOROLA	2N3904
846-01	388	.37	TRANSISTOR	2N3906
			MOTOROLA	2N3906
846-03	34	1.16	TRANSISTOR	2N4921
			MOTOROLA	2N4921
846-08	61	4.70	TRANSISTOR	2N4939
			MOTOROLA	2N4939
846-10	37	1.32	TRANSISTOR	2N4918
			MOTOROLA	2N4918
847-01	146	1.95	TRANSISTOR SELECTED	9934
			UNION CARBID	9934
847-12	32	11.25	TRANSISTOR	2N5516
			SILICONIX	2N5516
847-15	6	11.70	TRANSISTOR	2N5564
			SILICONIX	2N5564
847-19	2	7.35	TRANSISTOR	2N5912
			SILICONIX	2N5912
848-09	3	.92	INTEGRATED CIRCUIT	74H30
			ANY	74H30 (PLASTIC)
848-12	23	.70	INTEGRATED CIRCUIT	74H40
			ANY	74H40 (PLASTIC)
848-14	14	.92	INTEGRATED CIRCUIT	74H00
			ANY	74H00 (PLASTIC)

PART NO.	QTY	PRICE	DESCRIPTION
848-15	1	2.10	INTEGRATED CIRCUIT 74154
			ANY 74154 (ALT 9311)
848-16	3	1.04	INTEGRATED CIRCUIT 74H08
			ANY 74H08 (PLASTIC)
848-17	24	1.80	INTEGRATED CIRCUIT 74155
			ANY 74155 (PLASTIC)
848-23	4	3.33	INTEGRATED CIRCUIT MC3026P
			MOTOROLA MC3026P (PLASTIC)
848-24	21	1.12	INTEGRATED CIRCUIT 74H50
			ANY 74H50 (PLASTIC)
848-27	5	1.65	INTEGRATED CIRCUIT 7475
			ANY 7475 (PLASTIC)
848-28	5	1.20	INTEGRATED CIRCUIT 74H11
			ANY 74H11 (PLASTIC)
848-32	1	1.92	INTEGRATED CIRCUIT CA3019
			RCA CA3019 (MT CAN)
848-40	7	1.20	INTEGRATED CIRCUIT 74H04
			ANY 74H04 (PLASTIC)
848-48	13	.92	INTEGRATED CIRCUIT 74H10
			ANY 74H10 (PLASTIC)
848-58	6	1.50	INTEGRATED CIRCUIT 74157
			ANY 74157 (ALT 9322)
848-59	2	1.68	INTEGRATED CIRCUIT 74161
			ANY 74161 (ALT 9316)
848-60	2	.92	INTEGRATED CIRCUIT 7486
			ANY 7486 (PLASTIC)
848-65	5	1.32	INTEGRATED CIRCUIT MC1710CP
			MOTOROLA MC1710CP (PLASTIC)
848-77	5	1.80	INTEGRATED CIRCUIT 74H74
			ANY 74H74 (PLASTIC)
848-98	10	1.94	INTEGRATED CIRCUIT 8601
			ANY 8601 (ALT 9601)
849-36	13	1.71	INTEGRATED CIRCUIT 78M12UC
			FAIRCHILD 78M12UC (PLASTIC)
849-45	15	1.71	INTEGRATED CIRCUIT 78M15UC
			FAIRCHILD 78M15UC
849-46	52	2.64	INTEGRATED CIRCUIT LF356H
			NATIONAL LF356H (MT CAN)
849-47	13	1.71	INTEGRATED CIRCUIT 79M12UC
			FAIRCHILD 79M12UC
849-49	6	2.50	INTEGRATED CIRCUIT LF355H
			NATIONAL LF355H (MT CAN)
849-50	15	1.71	INTEGRATED CIRCUIT 79M15UC
			FAIRCHILD 79M15UC
849-64	13	.66	INTEGRATED CIRCUIT 74LS11
			ANY 74LS11 (PLASTIC)
851-00	1	.10	WASHER I.T. 3/8
			SMITH 1145
854-00	58	.02	WASHER FLAT #6 SM
			WALLACE NAS 620-C6

PART NO.	QTY	PRICE	DESCRIPTION
855-00	462	.03	WASHER FLAT #4 SM
			WALLACE NAS 620-C4
857-02	72	.06	WASHER FLAT #4 FIBRE
			SEASTROM 5602-10-32
859-00	13	.11	WASHER SHOULDER #4 NYLON
			SEASTROM 5607-10
859-01	1	.10	WASHER SHOULDER BUSHING NYLON
			BENDIX 2106307
859-02	7	.04	WASHER SHOULDER NYLON
			SEASTROM 5607-11
863-00	2	.02	WASHER E.T. #6
			WALLACE AN936-B6
863-02	2	.02	WASHER E.T. #8
			WALLACE AN936-B8
864-00	32	.01	WASHER E.T. # 10
			WALLACE AN936-B10
869-00	16	.02	WASHER FLAT #6 STD
			WALLACE AN960-C6
871-00	8	.03	WASHER FLAT #8
			WALLACE AN960-C8L
872-00	16	.03	WASHER FLAT #10
			WALLACE AN960-C10L
874-00	274	.01	WASHER LOCK #4
			WALLACE MS35337-78
876-00	3	.02	WASHER LOCK #8
			WALLACE MS35337-80
877-00	8	.02	WASHER LOCK #10
			WALLACE MS35337-81
972-02	1	41.20	CHASSIS SLIDE
			ZERO MFG C-300S-24-E98
998-07	2	5.00	RESISTOR .02% 796
			VISHAY V53-1-796
998-10	10	5.00	RESISTOR .02% 1K
			VISHAY V53-1-1K
998-15	2	5.00	RESISTOR .02% 1593.4
			VISHAY V53-1-1593.4
998-16	2	4.38	RESISTOR .02% 1587.7
			VISHAY V53-1-1587.7
998-20	1	2.37	RESISTOR .02% 1996
			VISHAY V53-1-1996
998-22	1	4.38	RESISTOR .02% 2K
			VISHAY V53-1-2K
998-24	2	4.38	RESISTOR .02% 3160
			VISHAY V53-1-3160
998-25	30	4.38	RESISTOR .02% 3988.4
			VISHAY V53-1-3988.4
998-26	2	5.00	RESISTOR .02% 3200
			VISHAY V53-1-3200
998-30	16	5.00	RESISTOR .02% 3992.4
			VISHAY V53-1-3992.4

PART NO.	QTY	PRICE	DESCRIPTION	
998-39	5	5.00	RESISTOR .02% 4K VISHAY V53-1-4K	
998-40	10	5.00	RESISTOR .02% 4008 VISHAY V53-1-4008	
998-42	2	4.00	RESISTOR .02% 4084 VISHAY V53-1-4084	
998-46	3	5.00	RESISTOR .02% 7993.6 VISHAY V53-1-7993.6	
998-47	5	5.00	RESISTOR .02% 8K VISHAY V53-1-8K	
998-53	32	4.00	RESISTOR .02% 10K VISHAY V53-1-10K	
998-85	64	5.70	RESISTOR .02% 45K VISHAY V53-1-45K	
999-24	20	4.38	RESISTOR .02% 398.84 VISHAY V53-1-398.84	
999-49	20	5.00	RESISTOR .02% 5K VISHAY V53-1-5K	
999-71	6	4.68	RESISTOR .02% 8032 VISHAY V53-1-8032	
999-87	40	4.38	RESISTOR .02% 50K VISHAY V53-1-50K	
9922-00	12	1.40	TRANSISTOR SELECT	A
9944-00	96	4.75	TRANSISTOR SELECT PAIR	A
9946-00	82	1.92	TRANSISTOR SELECT	A
9951-00	2	1.80	TRANSISTOR SELECT	A
9959-00	26	.00	INTEGRATED CIRCUIT OPAMP PAIR	A
9960-00	26	.00	INTEGRATED CIRCUIT SELECT	A
12018-01	1	.35	SHAFT EXTENDER	B
12027-00	1	.60	BRACE SINGLE POTENTIOMETER	B
30051-03	2	1.59	KNOB CONTROL	C
31818-00	1	1.96	BUSHING	B
40341-00	156	.41	GUIDE CARD	D
40454-00	2	10.00	COVER SIDE RIGHT & LEFT	D
40455-00	2	9.55	COVER TOP & BOTTOM	D
40456-02	1	10.00	PANEL REAR 2 AMP	A

PRICES SUBJECT TO CHANGE WITHOUT NOTICE

PART NO.	QTY	PRICE	DESCRIPTION	
40456-03	1	10.00	PANEL REAR 3 AMP	A
40457-00	10	3.75	SUPPORT INTERCONNECT	C
40461-00	23	.45	LENS LAMP	C
40461-02	1	.25	PLUG LAMP	C
40475-00	2	.30	PLUG SWITCH	C
46003-00	1	11.25	D&R ASSY AMP/LOGIC A-B	C
46019-00	2	11.25	D&R ASSY AMP LOGIC B	C
46020-00	1	7.85	SHIELD COMPONENT SIDE	C
46021-00	4	6.50	SHIELD CIRCUIT SIDE	B
46026-00	3	13.75	D&R ASSY AMP LOGIC C	C
46027-00	1	48.80	TRANSFORMER ASSY	C
46079-00	19	.80	HEATSINK	A
46123-00	1	13.75	D&R ASSY LOGIC BUFFER	C
46178-00	1	11.25	D&R ASSY 4 BIT LOGIC	C
48079-00	2	8.03	CABLE ASSY POWER	A
48088-00	1	30.00	D&R ASSY INTERCONN PWR SUP	C
48229-00	2	3.00	THERMOSTAT BRACKET	A
48289-00	2	18.75	D&R ASSY EXTENDER	C
50020-90	1	.00	RESISTOR .03% 222.22 PRESTON STYLE 18136	A
50040-25	4	2.70	RESISTOR .03% 1113.6 PRESTON STYLE 18136	A
50060-00	2	2.70	RESISTOR .03% 10K PRESTON STYLE 18136	A
50060-02	2	2.70	RESISTOR .03% 10.02K PRESTON STYLE 18136	A
50147-50	24	2.70	RESISTOR .03% 4K PRESTON STYLE 40350	A
50152-10	4	.00	RESISTOR .03% 6666.7 PRESTON STYLE 40350	A
50156-00	8	2.70	RESISTOR .03% 8K PRESTON STYLE 40350	A

PART NO.	QTY	PRICE	DESCRIPTION	
50159-99	26	.00	RESISTOR .03% 9990 PRESTON STYLE 40350	A
50160-00	16	2.70	RESISTOR .03% 10K PRESTON STYLE 40350	A
50160-08	26	.00	RESISTOR .03% 10.01K PRESTON STYLE 40350	A
51875-00	48	2.50	HEAT SINK	B
51982-00	2	17.00	PANEL SIDE	D
51983-00	2	8.75	COVER TOP & BOTTOM	D
52094-01	1	2.40	SHIELD PLATE	A
52099-00	1	3.75	TRANSFORMER ASSY	B
52184-00	10	7.85	SHIELD COMPONENT SIDE	C
52332-00	2	11.25	D&R ASSY SIGNAL BD EXTENDER	C
52383-00	1	13.75	D&R ASSY GMSH	C
52528-00	24	13.75	D&R ASSY 4 CHANNEL MUX	C
52533-00	1	13.75	D&R ASSY MUX COUNTER REG	C
52538-00	1	13.75	D&R ASSY ADC CONTROL	C
52548-00	1	13.75	D&R ASSY MUX DECODE 128 CHAN	C
52582-00	2	2.64	SWITCH ASSY MODE	A
52643-00	4	13.75	D&R ASSY AMP LOGIC A	C
52804-00	1	98.00	D&R ASSY INTERCONNECT BD A	C
52809-00	1	.00	MOD DWG CHASSIS SLIDE (PAIR)	A
53068-00	2	13.75	D&R ASSY GMD 10-1000	C
54278-00	1	.00	D&R ASSY AMP LOGIC ZCA	C
54283-00	1	.00	D&R ASSY ZERO CROSSING CONT	C
54528-00	13	.00	D&R ASSY DUAL GMD-1	C
55742-00	2	2.40	FEED THRU TERMINAL ASSY	B
56409-00	2	.80	TEMPERATURE INSULATOR	A

PART NO.	QTY	PRICE	DESCRIPTION	
56448-00	1	13.75	D&R ASSY BUFFER AMPLIFIER	C
56497-00	4	13.75	D&R ASSY GUARD DRIVER	C
56858-00	5	13.75	D&R ASSY DUAL GMD	C
58168-00	1	7.50	D&R ASSY LAMP DRIVER MUX	C
58488-00	1	13.75	D&R ASSY LOGIC BUFFER	C
58693-00	1	10.00	D&R ASSY LAMP DRIVER ADC	C
58705-00	1	16.25	PLATE CONNECTOR	B
58709-00	1	62.00	D&R ASSY INTERCONNECT BD C	C
58723-00	2	13.75	D&R ASSY GMD MUX AMPLIFIER	C
58837-00	1	.00	D&R ASSY INTERCONNECT BD A	C
58839-00	1	.00	D&R ASSY INTERCONNECT BD B	C
58844-00	1	16.25	PLATE CONNECTOR	B
58859-00	1	.00	D&R ASSY INTERCONNECT BD C	C
58908-00	2	13.75	D&R ASSY GMD AMP/MUX NOR IN	C
58934-00	1	.00	TRANSFORMER ASSY	C
58938-00	1	.00	D&R ASSY POWER SUPPLY	C
58968-00	2	13.75	D&R ASSY MUX CONTROL STORAGE	C
59008-00	1	13.75	D&R ASSY MUX CONTROL	C
59523-00	1	13.75	D&R ASSY 4 BIT AMP	C
59658-00	1	11.25	D&R ASSY REF SUPPLIES	C
59999-21	1	60.00	PANEL FRONT GMAD-1	D
59999-26	1	60.00	PANEL FRONT GMD	D

SECTION 11

DRAWINGS

Due to the size of the drawing package, the drawings describing the Part Number _____ are bound under separate cover.

SECTION 12

FACTORY TEST REPORT

PRESTON
SCIENTIFIC INCORPORATED
805 East Cerritos Ave., Anaheim, Calif. 92805
Tel. (714) 776-6400 TELEX 65-5321

MODEL GMAD-1

TEST REPORT

Test Technician Cheryl Brown

Date 8-18-78

Serial Number RAA990

Register Number 15967

1.0 Assembly number 58700-03

2.0 Resolution 14 Bits + Sign

3.0 Output code 2's Compliment

4.0 Output level for "1" +3v Nominal

5.0 Fullscale input ± 10.240 v FS

6.0 Number of counts ± 16384

7.0 Setup:

(a) +10 volt reference 9.9990

(b) Trigger slope POSITIVE

(c) Trigger level +3V NOMINAL

(d) Delay# _____ _____ nano/microseconds

(e) Delay# _____ _____ nano/micro seconds

(f) Delay# _____ _____ nano/micro seconds

8.0 Conversion time 5.4 usec

9.0 Throughput rate 222 KHz

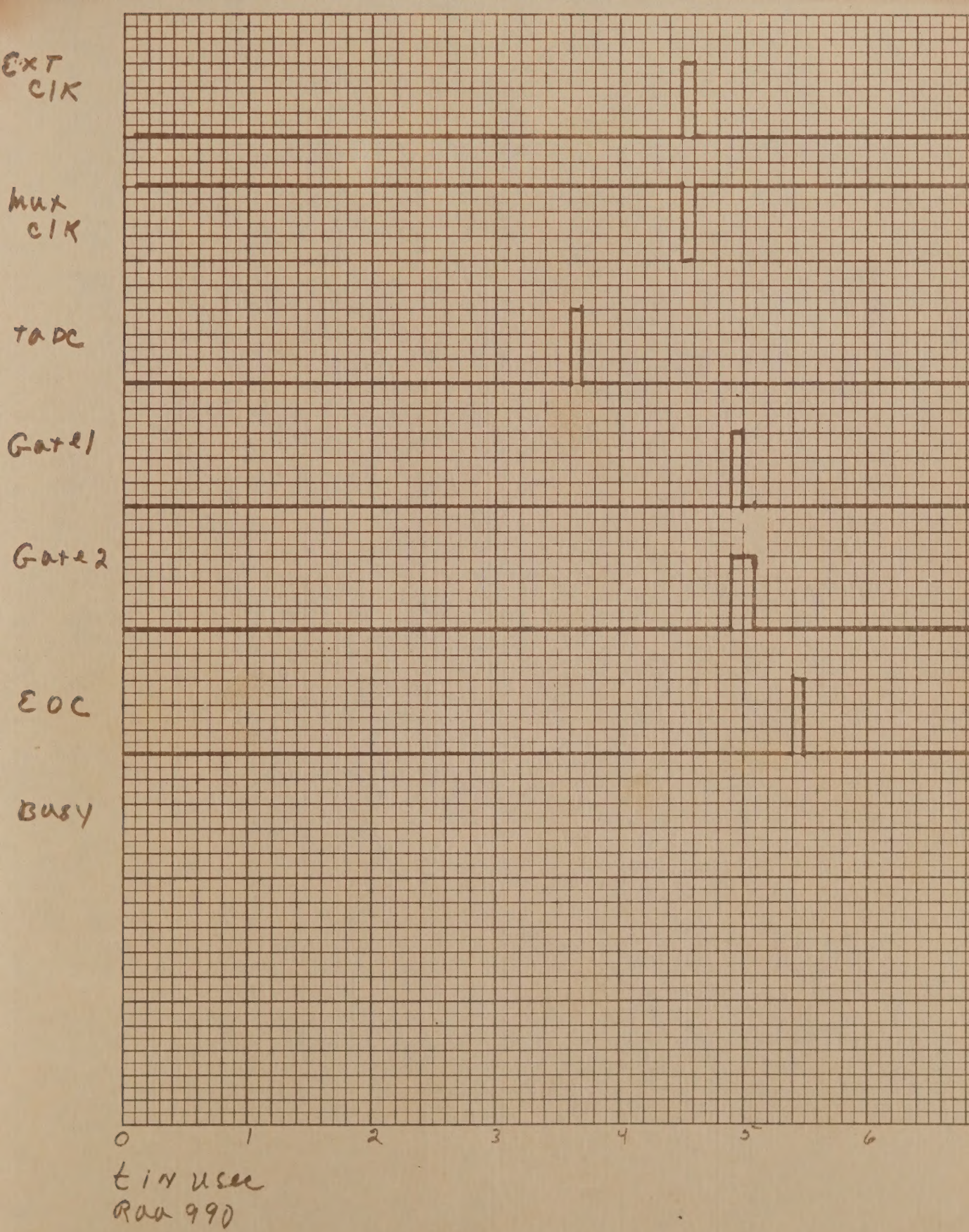
10.0 Accuracy ± .03% FS ± ½ LSB

11.0 Crossover check OK

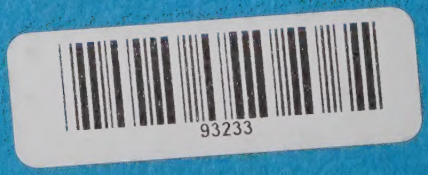
14 Bits & Sign
10.24v Full Scale

12.0 Binary Display (2's Compliment)	Theoretical Analog Input_____mv	Actual Analog Inputs	Error-The Minus Act
0 1 1 1 1 1 1 1 1 1 1 1 1 1 0	+ 10.2388	10.2392	+.4
0 1 1 1 1 0 0 0 0 0 0 0 0 0 0	+ 9.6000	9.6004	+.4
0 1 1 1 0 0 0 0 0 0 0 0 0 0 0	+ 8.9600	8.9605	+.5
0 1 1 0 0 0 0 0 0 0 0 0 0 0 0	+ 7.6800	7.6803	+.3
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	+ 5.1200	5.1205	+.5
0 0 0 1 0 0 0 0 0 0 0 0 0 0 0	+ 1.2800	1.2805	+.5
0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	+ .6400	0.6406	+.6
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	+ 0.0012	0.0015	+.3
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0.0000	-0.0003	-.3
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- 0.0006	0.0012	-.6
1 1 1 1 1 0 0 0 0 0 0 0 0 0 0	- .6400	0.6401	-.1
1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	- 1.2800	1.2800	0
1 1 1 0 0 0 0 0 0 0 0 0 0 0 0	- 2.5600	2.5601	-.1
1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	- 5.1200	5.1203	-.3
1 0 1 0 0 0 0 0 0 0 0 0 0 0 0	- 7.6800	7.6798	+.2
1 0 0 1 0 0 0 0 0 0 0 0 0 0 0	- 8.9600	8.9597	+.3
1 0 0 0 1 0 0 0 0 0 0 0 0 0 0	- 9.6000	9.5998	+.2
1 0 0 0 0 0 0 0 0 0 0 0 0 1 0	- 10.2388	10.2387	+.1

13.0 First reading error and crosstalk Less than ± 7 counts



Ran 990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